Application Brief 5.1A

Chipset simplifies Design of A/D Converter for PC-based Precision DVM Applications

Selecting Integration Time

For maximum 50/60 cycle line power noise rejection, Integration time t_{INT} must be picked as a multiple of the period of line power frequency. For example, t_{INT} times of 16.667 msec, 33.333 msec, 66.667 msec, 100 msec, 200 msec and 300 msec maximize 60 Hz line power noise rejection; and 20 msec, 50 msec, 100 msec, 200 msec and 300 msec maximize 50 Hz line power noise rejection. In general, the longer the integration time , the better the noise rejection of the line power noise, but it also takes longer to complete a conversion cycle. A default recommended integration time of 100 msec offer the best tradeoff between noise performance, conversion time and 50/60 cycle lin power noise rejection. The 100 msec integration time also offers the benefit of being universally optimal for both 50 cycle line power noise rejection and 60 cycle line power noise rejection.

Serial Data Transfer

The ALD521D has an internal 23 bit binary counter that can be clocked out serially at the end of an analog conversion cycle through an asynchronous handshake with an external processor. In addition, the ALD521D also determines the sign bit for the ALD500R, which is intended to be operated with bipolar power supplies. A logic 1 is a positive sign and a logic 0 is a negative sign. This sign bit is the 24 th bit being sent out by the ALD521D.

For each conversion cycle, the ALD521D send out a 24 bit serial word, which requires an external processor to send in 24 serial clock pulses. This 24 bit serial word consists of the content of a 23 bit binary counter, with the MSB being the first bit out, and the LSB being the second last bit out, followed by a sign bit as the last bit out. It signal a completed analog conversion cycle and readiness for the start of the serial data transfer by the transition of DVbar from a high to low state.

During a conversion cycle, the ALD521D keeps DVbar in a high, or logic 1, state. When the ALD521D has completed an analog conversion cycle, it sets the DVbar to low. Simultaneously, the ALD521D also put the first MSB bit of a 23 bit binary word, or bit 22, on Dout. An external processor can then read the data on Dout. For the first serial bit out, an external processor has a maximum of 5.5 msec to read this first bit and then send a serial clock pulse back to the ALD521D. This serial clock consists of a high to low transition, followed by a low to high transistion on SCLK. When the ALD521D has received an external serial clock on SCLK, it resets the DVbar to a high logic 1 state. Then it internally clocks the second bit, bit 21, onto the Dout, and sets the DVbar to a low state again. In this way, the ALD521D asynchronously transfer the 24 bit serial word to the external processor. The ALD521D continues to serially send out the remainder of the 24 bit data serially, when the last LSB binary bit, or bit 0, is followed by the sign bit.

When all 24 serial bits have been clocked out, the ALD521D then sets the DVbar to a high state, and starts the integration phase of the analog conversion cycle. It keeps DVbar high for the remainder four phases of the conversion cycle.

For an external processor to interface to the ALD521D, it need to have a minimum of 2 input pins and one output pin dedicated for the task. The ALD521D has DVbar (data valid), and Dout (data out) as outputs and SCLK (serial input clock) as input. The external processor can use either an interrupt or a data line for the interface to DVbar. After the ALD521D sends out the first DVbar high to low transition, it waits for a maximum of 5.5 milliseconds for an external serial clock at the SCLK input. If an external serial clock is not received during that time, the ALD521D times out internally, sets the DVbar to a high state, and start a new analog conversion cycle. For example, if an analog conversion cycle is equal to 200 msec., then DVbar would not become valid and effect a high to low transition again until 200 msec. later. The external processor can read DVbar as an interrupt to begin the serial clocking of the 24 bir data. The external processor can also sample DVbar as a data input, or it can synchronize to the A and B outputs of the ALD521D to determine when a serial word of an analog conversion may become available.

Interface to the ALD500R

The ALD521D has A and B outputs that control the four conversion phases of the ALD500/ALD500R, and it has Cout as an input from the ALD500/ALD500R. Note that Cout of the ALD500/ALD500R must be connected to pin 3 and pin 8 of the ALD521D. All the timing and control necessary between the ALD521D and the ALD500/ALD500R has been automated for continuous conversions.