Category: MOSFET

CIRCUIT IDEAS FOR DESIGNERS

Schematic no. fet_11103.0

Voltage Controlled Resistor

Description

This circuit shows an EPAD® MOSFET inverter circuit connected as a voltage controlled resistor circuit. The drain terminal is the output and the gate terminal is the input, which is connected to a voltage reference. The output voltage Vo is determined by the reference input voltage and the output loading R. The drain to source voltage and the drain current Ids forms one leg of a resistor divider, and the resistor R forms the other leg of the resistor divider. Depending on the value of R selected, the output Vo is biased in either negative tempco, zero tempco, or positive tempco modes. Note that the resistor R itself also contributes its own tempco term. This circuit works best when the Vo value is kept to a low level, such as at less than 1.0V. If a separate reference voltage is not available, a relatively stable voltage such as a regulated V+ or a voltage that is ratio-metric to V+ could be used, at increased Vo variations.

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