



Category: SABFET

CIRCUIT IDEAS FOR DESIGNERS

Schematic no. sabfet\_11104.0

**Balancing Two 2-Supercap (4 cell) Stacks in Series****Description**

Two dual supercapacitor auto balancing (SAB) MOSFET arrays connect across four-supercaps in series, using two separate packages of ALD 9100xx series, with xx equal to the threshold voltage,  $V_t$ , in 0.10V increments. At  $V_t$ , the  $I_{DS}$  ON current for each SAB MOSFET M1 and M2 for each stack is set at  $1\mu A$ . The  $I_{DS}$  ON current of each M1/M2 change exponentially with slight changes in the gate-source voltage,  $V_{GS}$ . Each SAB MOSFET  $M_x$  behaves like a voltage sensitive resistor (See sabfet\_11101.0). At  $V_{GS}$  voltages below or above  $V_t$ , the SAB MOSFET  $I_{DS}$  ON current changes at a rate of approximately 1 decade for every 0.1V change in  $V_{GS}$ . When  $V_{GS}$  drops low enough, the  $I_{DS}$  ON current becomes essentially zero. For example, the ALD910026 has a  $V_t$  of 2.60V. If its  $V_{GS}$  voltage falls below 2.0V, the  $I_{DS}$  current decreases to pA range, which is near zero compared to  $1\mu A$ .

The voltages across M1/M2 for each stack automatically self-adjust to accommodate different leakage currents for each supercap C1A/C2A/C1B/C2B.  $V_A$  settles to approximately  $\frac{1}{2}(V_+)$ , depending upon relative leakage currents of each supercap in both stacks. The currents through M1 and M2 for each stack automatically compensate for different supercap voltages. A higher supercap voltage results in a higher corresponding  $V_{GS}$  voltage of  $M_x$  connected across it, at a higher  $I_{DS}$  ON current, which opposes the tendency for the higher supercap voltage to increase. A lower supercap voltage results in lower  $I_{DS}$  ON currents in the corresponding SAB MOSFET until  $I_{DS}$  ON  $\approx 0$ . In equilibrium, the total leakage current across both M1/M2 and C1/C2 of each network is approximately equal to the highest leakage current of any one of C1A/C2A/C1B/C2B. Note that the absolute maximum voltage ratings must be observed for each individual SAB MOSFET package at all times.

For full schematic diagram and notes, please register and login at [aldinc.com](http://aldinc.com)