The ALD1105 is a monolithic dual N-channel and dual P-channel complementary matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices’ enhanced ACMOS silicon gate CMOS process. It consists of an ALD1116 N-channel MOSFET pair and an ALD1117 P-channel MOSFET pair in one package. The ALD1105 is a low drain current, low leakage current version of the ALD1103.

The ALD1105 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in ±2V to ±12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in complementary pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1105 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1105 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 30pA at room temperature. For example, DC beta of the device at a drain current of 3mA at 25°C is \( \frac{3mA}{30pA} = 100,000,000 \).

### Features
- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETs
- Low input capacitance
- Low Vos -- 10mV
- High input impedance -- \( 10^{15} \Omega \) typical
- Low input and output leakage currents
- Negative current (IDSS) temperature coefficient
- Enhancement mode (normally off)
- DC current gain 10^9
- Matched N-channel and matched P-channel in one package
- RoHS compliant

### Ordering Information

<table>
<thead>
<tr>
<th>Package</th>
<th>Pin Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBL, PBL, DB Packages</td>
<td><img src="image" alt="Pin Configuration Diagram" /></td>
</tr>
</tbody>
</table>

**Operating Temperature Range**

<table>
<thead>
<tr>
<th>Package</th>
<th>Operating Temperature Range*</th>
</tr>
</thead>
<tbody>
<tr>
<td>14-Pin Small Outline Plastic Dip Package (SOIC)</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>ALD1105SBL ALD1105PBL ALD1105DB</td>
<td>0°C to +70°C</td>
</tr>
</tbody>
</table>

* Contact factory for leaded (non-RoHS) or high temperature versions.

**Applications**
- Precision current mirrors
- Complementary push-pull linear drives
- Analog switches
- Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog inverter
- Precision matched current sources

**Block Diagram**

![Block Diagram](image)

**Features**
- Thermal tracking between N-channel and P-channel pairs
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</tr>
</tbody>
</table>

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ABSOLUTE MAXIMUM RATINGS

Drain-source voltage, \( V_{DS} \) .......................................................... 10.6V
Gate-source voltage, \( V_{GS} \) .......................................................... 10.6V
Power dissipation ........................................................................... 500mW
Operating temperature range  SBL, PBL packages ................................... 0°C to +70°C
                                      DB package .................................................. -55°C to +125°C
Storage temperature range ........................................................... -65°C to +150°C
Lead temperature, 10 seconds ...................................................... +260°C
CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS
\( T_A = 25°C \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Threshold Voltage</td>
<td>( V_T )</td>
<td>0.4</td>
<td>0.7</td>
<td>1.0</td>
<td>V</td>
<td>( I_{DS} = 1\mu A ) ( V_{GS} = V_{DS} )</td>
<td>-0.4</td>
<td>-0.7</td>
<td>-1.0</td>
<td>V</td>
<td>( I_{DS} = -1\mu A ) ( V_{GS} = V_{DS} )</td>
</tr>
<tr>
<td>Offset Voltage ( V_{GS1} - V_{GS2} )</td>
<td>( V_{OS} )</td>
<td>2</td>
<td>10</td>
<td>mV</td>
<td>( I_{DS} = 10\mu A ) ( V_{GS} = V_{DS} )</td>
<td>2</td>
<td>10</td>
<td>mV</td>
<td>( I_{DS} = -10\mu A ) ( V_{GS} = V_{DS} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Threshold Temperature Drift</td>
<td>( T_{CV_T} )</td>
<td>-1.2</td>
<td>mV/°C</td>
<td>-1.3</td>
<td>mV/°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On Drain Current</td>
<td>( I_{DS(ON)} )</td>
<td>3</td>
<td>4.8</td>
<td>mA</td>
<td>( V_{GS} = V_{DS} = 5V )</td>
<td>-1.3</td>
<td>-2</td>
<td>mA</td>
<td>( V_{GS} = V_{DS} = -5V )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Trans-conductance</td>
<td>( G_S )</td>
<td>1</td>
<td>1.8</td>
<td>mmho</td>
<td>( V_{DS} = 5V ) ( I_{DS} = 10mA )</td>
<td>0.25</td>
<td>0.67</td>
<td>mmho</td>
<td>( V_{DS} = -5V ) ( I_{DS} = -10mA )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mismatch</td>
<td>( \Delta G_S )</td>
<td>0.5</td>
<td>%</td>
<td>0.5</td>
<td>%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Conductance</td>
<td>( G_{OS} )</td>
<td>200</td>
<td>( \mu mho )</td>
<td>40</td>
<td>( \mu mho )</td>
<td>( V_{DS} = 5V ) ( I_{DS} = 10mA )</td>
<td>( V_{DS} = -5V ) ( I_{DS} = -10mA )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain Source ON Resistance</td>
<td>( R_{DS(ON)} )</td>
<td>350</td>
<td>500</td>
<td>( \Omega )</td>
<td>( V_{DS} = 0.1V ) ( V_{GS} = 5V )</td>
<td>1200</td>
<td>1800</td>
<td>( \Omega )</td>
<td>( V_{DS} = 0.1V ) ( V_{GS} = -5V )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain Source ON Resistance Mismatch</td>
<td>( \Delta R_{DS(ON)} )</td>
<td>0.5</td>
<td>%</td>
<td>0.5</td>
<td>%</td>
<td>( V_{DS} = 0.1V ) ( V_{GS} = 5V )</td>
<td>( V_{DS} = 0.1V ) ( V_{GS} = -5V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain Source Breakdown Voltage</td>
<td>( B_{VDSS} )</td>
<td>12</td>
<td>V</td>
<td>( I_{DS} = 1\mu A ) ( V_{GS} = 0V )</td>
<td>-12</td>
<td>V</td>
<td>( I_{DS} = -1\mu A ) ( V_{GS} = 0V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Off Drain Current</td>
<td>( I_{DS(OFF)} )</td>
<td>10</td>
<td>400</td>
<td>pA</td>
<td>( V_{DS} = 12V ) ( I_{GS} = 0V )</td>
<td>10</td>
<td>400</td>
<td>pA</td>
<td>( V_{DS} = 12V ) ( I_{GS} = 0V )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Leakage Current</td>
<td>( I_{GS} )</td>
<td>0.1</td>
<td>30</td>
<td>pA</td>
<td>( V_{DS} = 0V ) ( V_{GS} = 12V )</td>
<td>1</td>
<td>30</td>
<td>pA</td>
<td>( V_{DS} = 0V ) ( V_{GS} = 12V )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>( C_{ISS} )</td>
<td>1</td>
<td>3</td>
<td>pF</td>
<td>1</td>
<td>3</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
TYPICAL P-CHANNEL PERFORMANCE CHARACTERISTICS

OUTPUT CHARACTERISTICS

DRAIN SOURCE VOLTAGE (V)

DRAIN SOURCE CURRENT (mA)

VBS = 0V
T_A = 25°C
Vgs = -12V
-10V
-8V
-6V
-4V
-2V

VBS = 0V
T_A = 25°C
Vgs = -12V
-10V
-8V
-6V
-4V
-2V

LOW VOLTAGE OUTPUT CHARACTERISTICS

DRAIN SOURCE VOLTAGE (mV)

DRAIN SOURCE CURRENT (µA)

VBS = 0V
T_A = 25°C
Vgs = -12V
-10V
-8V
-6V
-4V
-2V

VBS = 0V
T_A = 25°C
Vgs = -12V
-10V
-8V
-6V
-4V
-2V

FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE

FORWARD TRANSCONDUCTANCE (mmho)

VBS = 0V
f = 1KHz
IDS = -5mA

VBS = 0V
f = 1KHz
IDS = -1mA

TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS

DRAIN SOURCE CURRENT (µA)

VBS = 0V
VGS = VDS
T_A = 25°C
4V
6V
8V
10V
12V

VBS = 0V
VGS = VDS
T_A = 25°C
4V
6V
8V
10V
12V

DRAIN SOURCE ON RESISTANCE

R_DS (ON) vs. GATE SOURCE VOLTAGE

DRAIN SOURCE ON RESISTANCE (KΩ)

VDS = 0.4V
VBS = 0V

T_A = +125°C

VDS = -12V
VBS = 0V

VDS = -12V
VBS = 0V

OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE

OFF DRAIN SOURCE CURRENT (pA)

AMBENT TEMPERATURE (°C)
TYPICAL N-CHANNEL PERFORMANCE CHARACTERISTICS

**OUTPUT CHARACTERISTICS**

- **DRAIN SOURCE CURRENT (mA)**
  - $V_{BS} = 0V$
  - $V_{GS} = 12V$
  - $10V$
  - $8V$
  - $6V$
  - $4V$
  - $2V$

- **DRAIN SOURCE VOLTAGE (V)**
  - $V_{BS} = 0V$
  - $V_{GS} = 12V$

- **TA = 25°C**

**LOW VOLTAGE OUTPUT CHARACTERISTICS**

- **DRAIN SOURCE CURRENT (µA)**
  - $-160$ - $80$ - $0$ - $80$ - $160$
  - $-1000$ - $500$ - $0$ - $500$
  - $4V$
  - $V_{GS} = 12V$

- **DRAIN SOURCE VOLTAGE (mV)**
  - $-1000$ - $-800$ - $0$ - $800$ - $1000$
  - $V_{BS} = 0V$

**FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE**

- **FORWARD TRANSCONDUCTANCE (mmho)**
  - $20$ - $10$ - $5$ - $1$
  - $0.5$

- **DRAIN SOURCE VOLTAGE (V)**
  - $20$ - $10$ - $2$

- **TA = +125°C**

**TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS**

- **DRAIN SOURCE CURRENT (µA)**
  - $20$ - $15$ - $10$ - $5$

- **GATE SOURCE VOLTAGE (V)**
  - $0$ - $0.8$ - $1.6$ - $2.4$ - $3.2$ - $4.0$

- **TA = 25°C**

**DRAIN SOURCE ON RESISTANCE $R_{DS(ON)}$ vs. GATE SOURCE VOLTAGE**

- **DRAIN SOURCE ON RESISTANCE (KΩ)**
  - $100$ - $10$ - $1$

- **GATE SOURCE VOLTAGE (V)**
  - $V_{DS} = 0.2V$
  - $V_{GS} = 0V$

- **TA = +125°C**

**OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE**

- **OFF DRAIN SOURCE CURRENT (pA)**
  - $-50$ - $-25$ - $+25$ - $+50$ - $+75$ - $+125$

- **AMBIENT TEMPERATURE (°C)**
  - $V_{DS} = +12V$
  - $V_{GS} = V_{BS} = 0V$

**OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE**

- **OFF DRAIN SOURCE CURRENT (pA)**
  - $1000$

- **AMBIENT TEMPERATURE (°C)**
  - $-50$ - $-25$ - $0$ - $+25$ - $+50$ - $+75$ - $+100$ - $+125$
TYPICAL APPLICATIONS

CURRENT SOURCE MIRROR

\[ I_{\text{SOURCE}} = I_{\text{SET}} \]

\[ R_{\text{SET}} = \frac{V^+ - V_t}{4} \]

Q1, Q2: N-channel MOSFET
Q3, Q4: P-channel MOSFET

CURRENT SOURCE WITH GATE CONTROL

Digital Logic Control of Current Source

Q1: N-channel MOSFET
Q3, Q4: P-channel MOSFET

DIFFERENTIAL AMPLIFIER

\[ V_{\text{OUT}} = \frac{V_{\text{IN}^+} - V_{\text{IN}^-}}{R_{\text{PMOS}}} \]

\[ R_{\text{PMOS}} = R_{\text{NMOS}} \]

Q1, Q2: N-channel MOSFET
Q3, Q4: P-channel MOSFET

CURRENT SOURCE MULTIPLICATION

\[ I_{\text{SOURCE}} = I_{\text{SET}} \times N \]

Q1, Q2, Q3, Q4: P-channel MOSFET
QSET, Q1, QN: ALD 1106 or ALD 1105
N: N-channel MOSFET
TYPICAL APPLICATIONS (cont.)

BASIC CURRENT SOURCES

N-CHANNEL CURRENT SOURCE

\[ I_{\text{SOURCE}} = I_{\text{SET}} = \frac{V^+ - V_t}{R_{\text{SET}}} \approx \frac{V^+ - 1.0}{R_{\text{SET}}} = \frac{4}{R_{\text{SET}}} \]

Q1, Q2: N-Channel MOSFET

P-CHANNEL CURRENT SOURCE

\[ I_{\text{SOURCE}} = I_{\text{SET}} = \frac{V^+}{R_{\text{SET}}} \]

Q3, Q4: P-Channel MOSFET

CASCODE CURRENT SOURCES

\[ I_{\text{SOURCE}} = I_{\text{SET}} = \frac{V^+ - 2V_t}{R_{\text{SET}}} \approx \frac{3}{R_{\text{SET}}} \]

Q1, Q2, Q3, Q4: N-Channel MOSFET

(1/2 ALD1105 + ALD1116)

Q1, Q2, Q3, Q4: P-Channel MOSFET

(1/2 ALD1105 + ALD1117)
### SOIC-14 PACKAGE DRAWING

**14 Pin Plastic SOIC Package**

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.35 - 1.75</td>
<td>0.053 - 0.069</td>
</tr>
<tr>
<td>A₁</td>
<td>0.10 - 0.25</td>
<td>0.004 - 0.010</td>
</tr>
<tr>
<td>b</td>
<td>0.35 - 0.45</td>
<td>0.014 - 0.018</td>
</tr>
<tr>
<td>C</td>
<td>0.18 - 0.25</td>
<td>0.007 - 0.010</td>
</tr>
<tr>
<td>D-14</td>
<td>8.55 - 8.75</td>
<td>0.336 - 0.345</td>
</tr>
<tr>
<td>E</td>
<td>3.50 - 4.05</td>
<td>0.140 - 0.160</td>
</tr>
<tr>
<td>e</td>
<td>1.27 BSC</td>
<td>0.050 BSC</td>
</tr>
<tr>
<td>H</td>
<td>5.70 - 6.30</td>
<td>0.224 - 0.248</td>
</tr>
<tr>
<td>L</td>
<td>0.60 - 0.937</td>
<td>0.024 - 0.037</td>
</tr>
<tr>
<td>Ø</td>
<td>0° - 8°</td>
<td>0° - 8°</td>
</tr>
<tr>
<td>S</td>
<td>0.25 - 0.50</td>
<td>0.010 - 0.020</td>
</tr>
</tbody>
</table>

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*ALD1105 Advanced Linear Devices 7 of 9*
# PDIP-14 PACKAGE DRAWING

## 14 Pin Plastic DIP Package

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.81 - 5.08</td>
<td>0.105 - 0.200</td>
</tr>
<tr>
<td>A1</td>
<td>0.38 - 1.27</td>
<td>0.015 - 0.050</td>
</tr>
<tr>
<td>A2</td>
<td>1.27 - 2.03</td>
<td>0.050 - 0.080</td>
</tr>
<tr>
<td>b</td>
<td>0.89 - 1.65</td>
<td>0.035 - 0.065</td>
</tr>
<tr>
<td>b1</td>
<td>0.38 - 0.51</td>
<td>0.015 - 0.020</td>
</tr>
<tr>
<td>c</td>
<td>0.20 - 0.30</td>
<td>0.008 - 0.012</td>
</tr>
<tr>
<td>D</td>
<td>17.27 - 19.30</td>
<td>0.680 - 0.760</td>
</tr>
<tr>
<td>E</td>
<td>5.59 - 7.11</td>
<td>0.220 - 0.280</td>
</tr>
<tr>
<td>E1</td>
<td>7.62 - 8.26</td>
<td>0.300 - 0.325</td>
</tr>
<tr>
<td>e</td>
<td>2.29 - 2.79</td>
<td>0.090 - 0.110</td>
</tr>
<tr>
<td>e1</td>
<td>7.37 - 7.87</td>
<td>0.290 - 0.310</td>
</tr>
<tr>
<td>L</td>
<td>2.79 - 3.81</td>
<td>0.110 - 0.150</td>
</tr>
<tr>
<td>S</td>
<td>1.02 - 2.03</td>
<td>0.040 - 0.080</td>
</tr>
<tr>
<td>ø</td>
<td>0° - 15°</td>
<td>0° - 15°</td>
</tr>
</tbody>
</table>
CERDIP-14 PACKAGE DRAWING

14 Pin CERDIP Package

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.55</td>
<td>0.140</td>
</tr>
<tr>
<td>A1</td>
<td>1.27</td>
<td>0.050</td>
</tr>
<tr>
<td>b</td>
<td>0.97</td>
<td>0.038</td>
</tr>
<tr>
<td>b1</td>
<td>0.36</td>
<td>0.014</td>
</tr>
<tr>
<td>C</td>
<td>0.20</td>
<td>0.008</td>
</tr>
<tr>
<td>D-14</td>
<td>--</td>
<td>0.785</td>
</tr>
<tr>
<td>E</td>
<td>5.59</td>
<td>0.220</td>
</tr>
<tr>
<td>E1</td>
<td>7.73</td>
<td>0.290</td>
</tr>
<tr>
<td>e</td>
<td>2.54 BSC</td>
<td>0.100 BSC</td>
</tr>
<tr>
<td>e1</td>
<td>7.62 BSC</td>
<td>0.300 BSC</td>
</tr>
<tr>
<td>L</td>
<td>3.81</td>
<td>0.150</td>
</tr>
<tr>
<td>L1</td>
<td>3.18</td>
<td>0.125</td>
</tr>
<tr>
<td>L2</td>
<td>0.38</td>
<td>0.015</td>
</tr>
<tr>
<td>S</td>
<td>--</td>
<td>2.49</td>
</tr>
<tr>
<td>Ø</td>
<td>0°</td>
<td>15°</td>
</tr>
</tbody>
</table>