



**QUAD/DUAL N-CHANNEL ENHANCEMENT MODE EPAD®
MATCHED PAIR MOSFET ARRAY**

$V_{GS(th)} = +0.4V$

GENERAL DESCRIPTION

ALD110804/ALD110904 are monolithic quad/dual N-Channel MOSFETs matched at the factory using ALD's proven EPAD® CMOS technology. These devices are intended for low voltage, small signal applications. The ALD110804/ALD110904 MOSFETs are designed and built for exceptional device electrical characteristics matching. Since these devices are on the same monolithic chip, they also exhibit excellent tempco tracking characteristics. They are versatile circuit elements useful as design components for a broad range of analog applications, such as basic building blocks for current sources, differential amplifier input stages, transmission gates, and multiplexer applications. For most applications, connect V⁻ and N/C pins to the most negative voltage potential in the system and V⁺ pin to the most positive voltage potential (or left open unused). All other pins must have voltages within these voltage limits.

The ALD110804/ALD110904 devices are built for minimum offset voltage and differential thermal response, and they are suited for switching and amplifying applications in <+0.1V to +10V systems where low input bias current, low input capacitance and fast switching speed are desired, as these devices exhibit well controlled turn-off and sub-threshold characteristics and can be biased and operated in the sub-threshold region. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment.

The ALD110804/ALD110904 are suitable for use in very low operating voltage or very low power (nanowatt), precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result from extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 30pA at room temperature. For example, DC beta of the device at a drain current of 3mA and input leakage current of 30pA at 25°C is $= 3mA/30pA = 100,000,000$.

FEATURES

- Enhancement-mode (normally off)
- Precision Gate Threshold Voltage of +0.40V
- Matched MOSFET to MOSFET characteristics
- Tight lot to lot parametric control
- Low input capacitance
- $V_{GS(th)}$ match (V_{OS}) to 10mV
- High input impedance — $10^{12}\Omega$ typical
- Positive, zero, and negative $V_{GS(th)}$ temperature coefficient
- DC current gain $>10^8$
- Low input and output leakage currents

ORDERING INFORMATION

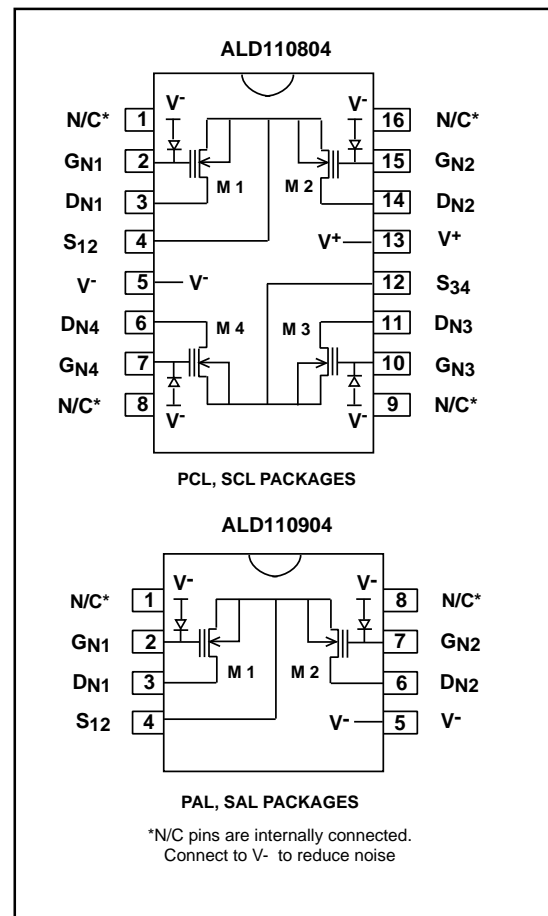
Operating Temperature Range*		Operating Temperature Range*	
0°C to +70°C		0°C to +70°C	
16-Pin Plastic Dip Package	16-Pin SOIC Package	8-Pin Plastic Dip Package	8-Pin SOIC Package
ALD110804PCL	ALD110804SCL	ALD110904PAL	ALD110904SAL

* Contact factory for industrial or military temp. ranges or user-specified threshold voltage values.

APPLICATIONS

- Ultra low power (nanowatt) analog and digital circuits
- Ultra low operating voltage (<0.4V) circuits
- Sub-threshold biased and operated circuits
- Precision current mirrors and current sources
- Nano-Amp current sources
- High impedance resistor simulators
- Capacitive probes and sensor interfaces
- Differential amplifier input stages
- Discrete Voltage comparators and level shifters
- Voltage bias circuits
- Sample and Hold circuits
- Analog and digital inverters
- Charge detectors and charge integrators
- Source followers and High Impedance buffers
- Current multipliers
- Discrete Analog switches / multiplexers

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Drain-Source voltage, V_{DS}	10.6V
Gate-Source voltage, V_{GS}	10.6V
Power dissipation	500 mW
Operating temperature range PA, SA, PC, SC package	0°C to +70°C
Storage temperature range	-65°C to +150°C
Lead temperature, 10 seconds	+260°C

OPERATING ELECTRICAL CHARACTERISTICS

$V_+ = +5V$ (or open) $V_- = GND$ $T_A = 25^\circ C$ unless otherwise specified

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

Parameter	Symbol	ALD110804 / ALD110904			Unit	Test Conditions
		Min	Typ	Max		
Gate Threshold Voltage	$V_{GS(th)}$	0.38	0.40	0.42	V	$I_{DS} = 1\mu A$ $V_{DS} = 0.1V$
Offset Voltage $V_{GS(th)1} - V_{GS(th)2}$	V_{OS}		2	10	mV	
Offset Voltage Tempco	$TC \Delta V_{OS}$		5		$\mu V / ^\circ C$	$V_{DS1} = V_{DS2}$
Gate Threshold Voltage Tempco	$TC \Delta V_{GS(th)}$		-1.7 0.0 +1.6		$mV / ^\circ C$	$I_D = 1\mu A$ $I_D = 20\mu A, V_{DS} = 0.1V$ $I_D = 40\mu A$
On Drain Current	$I_{DS(ON)}$		12.0 3.0		mA	$V_{GS} = +9.9V$ $V_{GS} = +4.2V$ $V_{DS} = +5V$
Forward Transconductance	GFS		1.4		mmho	$V_{GS} = +4.4V$ $V_{DS} = +9.4V$
Transconductance Mismatch	ΔGFS		1.8		%	
Output Conductance	GOS		68		μmho	$V_{GS} = +4.4V$ $V_{DS} = +9.4V$
Drain Source On Resistance	$R_{DS(ON)}$		500		Ω	$V_{DS} = 0.1V$ $V_{GS} = +4.4V$
Drain Source On Resistance Mismatch	$\Delta R_{DS(ON)}$		0.5		%	
Drain Source Breakdown Voltage	BV_{DSX}		10		V	$I_{DS} = 1.0\mu A$ $V_{GS} = -0.6V$
Drain Source Leakage Current ¹	$I_{DS(OFF)}$		10	100 4	pA nA	$V_{GS} = -0.6V$ $V_{DS} = 10V, T_A = 125^\circ C$
Gate Leakage Current ¹	I_{GSS}		3	30 1	pA nA	$V_{DS} = 0V, V_{GS} = 10V$ $T_A = 125^\circ C$
Input Capacitance	C_{ISS}		2.5		pF	
Transfer Reverse Capacitance	C_{RSS}		0.1		pF	
Turn-on Delay Time	t_{on}		10		ns	$V_+ = 5V, R_L = 5K\Omega$
Turn-off Delay Time	t_{off}		10		ns	$V_+ = 5V, R_L = 5K\Omega$
Crosstalk			60		dB	$f = 100KHz$

Notes: ¹ Consists of junction leakage currents