GENERAL DESCRIPTION

The ALD1115 is a monolithic complementary N-channel and P-channel transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of a N-channel MOSFET and a P-channel MOSFET in one package. The ALD1115 is a dual version of the quad complementary ALD1105.

The ALD1115 offers high input impedance and negative current temperature coefficient. The transistor pair is designed for precision signal switching and amplifying applications in +1V to +10V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When connected in parallel with sources, drains and gates connected together, a CMOS analog switch can be constructed. In addition, the ALD1115 is intended as a building block for CMOS inverters, differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1115 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 100pA at room temperature. V+ is connected to the substrate, which is the most positive voltage potential of the ALD1115, usually SP (5). Similarly, V- is connected to the most negative voltage potential of the ALD1115, usually SN (1).

FEATURES

- Thermal tracking between N-channel and P-channel
- Low threshold voltage of 0.7V for both N-channel and P-channel MOSFETs
- Low input capacitance
- High input impedance -- \(10^{13}\Omega\) typical
- Low input and output leakage currents
- Negative current (IDSS) temperature coefficient
- Enhancement-mode (normally off)
- DC current gain \(10^9\)
- Single N-channel MOSFET and single P-channel MOSFET in one package

APPLICATIONS

- Precision current mirrors
- Complementary push-pull linear drives
- Discrete analog switches
- Analog signal choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog current inverter
- Precision matched current sources
- CMOS inverter stage
- Diode clamps
- Source followers

PIN CONFIGURATION

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SN</td>
</tr>
<tr>
<td>2</td>
<td>GN</td>
</tr>
<tr>
<td>3</td>
<td>DN</td>
</tr>
<tr>
<td>4</td>
<td>V-</td>
</tr>
<tr>
<td>5</td>
<td>SP</td>
</tr>
<tr>
<td>6</td>
<td>GP</td>
</tr>
<tr>
<td>7</td>
<td>DP</td>
</tr>
<tr>
<td>8</td>
<td>V+</td>
</tr>
</tbody>
</table>

TOP VIEW
SAL, PAL PACKAGES

ORDERING INFORMATION (*“L” suffix denotes lead-free (RoHS))*

<table>
<thead>
<tr>
<th>Package</th>
<th>Operating Temperature Range*</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Pin SOIC Plastic Dip Package</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>ALD1115SAL ALD1115PAL</td>
<td></td>
</tr>
</tbody>
</table>

* Contact factory for high temperature versions.
### ABSOLUTE MAXIMUM RATINGS
- Drain-source voltage, $V_{DS}$: 10V
- Gate-source voltage, $V_{GS}$: 10V
- Power dissipation: 500mW
- Operating temperature range: 0°C to +70°C
- Storage temperature range: -65°C to +150°C
- Lead temperature, 10 seconds: +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

### OPERATING ELECTRICAL CHARACTERISTICS
$T_A = 25^\circ C$ unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>N - Channel</th>
<th>Test Conditions</th>
<th>P - Channel</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Threshold Voltage</td>
<td>$V_T$</td>
<td>0.4</td>
<td>0.7</td>
<td>1.0 V</td>
<td>$I_DS = 1\mu A$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>Gate Threshold Temperature Drift</td>
<td>$T_{CVT}$</td>
<td>-1.2 mV/°C</td>
<td></td>
<td></td>
<td>-1.3 mV/°C</td>
</tr>
<tr>
<td>On Drain Current</td>
<td>$I_DS(ON)$</td>
<td>3 mA</td>
<td>4.8 mA</td>
<td>$V_{GS} = V_{DS} = 5V$</td>
<td>-1.3 mA</td>
</tr>
<tr>
<td>Trans.-conductance</td>
<td>$G_{ds}$</td>
<td>1 mmho</td>
<td>1.8 mmho</td>
<td>$V_{DS} = 5V$</td>
<td>$I_DS = 10mA$</td>
</tr>
<tr>
<td>Output Conductance</td>
<td>$G_{OS}$</td>
<td>200 mmho</td>
<td>40 mmho</td>
<td>$V_{DS} = 5V$</td>
<td>$I_DS = 10mA$</td>
</tr>
<tr>
<td>Drain Source ON Resistance</td>
<td>$R_{DS(ON)}$</td>
<td>350 Ω</td>
<td>500 Ω</td>
<td>$V_{DS} = 0.1V$</td>
<td>$V_{GS} = 5V$</td>
</tr>
<tr>
<td>Drain Source Breakdown Voltage</td>
<td>$BVDSS$</td>
<td>10 V</td>
<td>$I_DS = 1\mu A$</td>
<td>$V_{GS} = 0V$</td>
<td>-10 V</td>
</tr>
<tr>
<td>Off Drain Current</td>
<td>$I_DS(OFF)$</td>
<td>10 pA</td>
<td>400 pA</td>
<td>$V_{DS} = 10V$</td>
<td>$I_{GS} = 0V$</td>
</tr>
<tr>
<td>Gate Leakage Current</td>
<td>$I_{GSS}$</td>
<td>1 pA</td>
<td>100 pA</td>
<td>$V_{DS} = 0V$</td>
<td>$V_{GS} = 10V$</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>$C_{ISS}$</td>
<td>1 pF</td>
<td>3 pF</td>
<td>$V_{GS} = 0V$</td>
<td>$V_{DS} = 10V$</td>
</tr>
</tbody>
</table>
TYPICAL N-CHANNEL PERFORMANCE CHARACTERISTICS

OUTPUT CHARACTERISTICS

DRAIN SOURCE ON CURRENT

\[ I_{DS(ON)} \text{ (mA)} \]

\[ V_{DS(ON)} \text{ (V)} \]

\[ V_{BS} = 0V \]

\[ V_{GS} = 10V \]

\[ V_{BS} = 0V \]

\[ V_{GS} = 10V \]

\[ T_A = +25^\circ C \]

\[ 8V \]

\[ 6V \]

\[ 4V \]

\[ 2V \]

DRAIN SOURCE ON VOLTAGE

\[ V_{DS(ON)} \text{ (mV)} \]

\[ V_{BS} = 0V \]

\[ V_{GS} = 10V \]

\[ V_{BS} = 0V \]

\[ V_{GS} = 10V \]

\[ T_A = +25^\circ C \]

\[ 8V \]

\[ 6V \]

\[ 4V \]

\[ 2V \]

FORWARD TRANSCONDUCTANCE vs.
DRAIN-SOURCE VOLTAGE

FORWARD TRANSCONDUCTANCE

\[ (\text{mmho}) \]

\[ V_{BS} = 0V \]

\[ f = 1\text{KHz} \]

\[ V_{BS} = 0V \]

\[ V_{GS} = V_{DS} \]

\[ T_A = +25^\circ C \]

\[ 10mA \]

\[ 1mA \]

\[ 100 \]

\[ 10 \]

\[ 1 \]

\[ 0.1 \]

DRAIN SOURCE ON RESISTANCE vs.
GATE-SOURCE VOLTAGE

DRAIN SOURCE OFF CURRENT vs.
AMBIENT TEMPERATURE

DRAIN SOURCE OFF CURRENT

\[ (\text{pA}) \]

\[ V_{BS} = 0V \]

\[ V_{GS} = 10V \]

\[ T_A = +25^\circ C \]

\[ -50 \]

\[ -25 \]

\[ 0 \]

\[ +25 \]

\[ +50 \]

\[ +125 \]

\[ +100 \]

\[ +75 \]

\[ +50 \]

\[ +25 \]

\[ +125 \]

\[ +100 \]

\[ +75 \]

\[ +50 \]

\[ +25 \]

\[ +125 \]

\[ +100 \]

\[ +75 \]

\[ +50 \]

\[ +25 \]

\[ +125 \]

\[ +100 \]

\[ +75 \]

\[ +50 \]

\[ +25 \]
TYPICAL P-CHANNEL PERFORMANCE CHARACTERISTICS

OUTPUT CHARACTERISTICS

LOW VOLTAGE OUTPUT CHARACTERISTICS

TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS

FORWARD TRANSDUCTANCE vs. DRAIN-SOURCE VOLTAGE

TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS

DRAIN SOURCE ON RESISTANCE vs. GATE-SOURCE VOLTAGE

DRAIN SOURCE OFF CURRENT vs. AMBIENT TEMPERATURE
TYPICAL APPLICATIONS

CURRENT SOURCE MIRROR

$\text{ISOURCE} = \frac{V^+ - V_t}{R_{\text{set}}}$

$Q_1, Q_2$: N-Channel MOSFET

$Q_3, Q_4$: P-Channel MOSFET

CURRENT SOURCE WITH GATE CONTROL

$\text{ISOURCE} = \frac{\text{ISET}}{4}$

Q1, Q2: N-Channel MOSFET

Q3, Q4: P-Channel MOSFET

CMOS INVERTER

CMOS ANALOG SWITCH
TYPICAL APPLICATIONS (cont.)

DIODE-CONNECTED CONFIGURATION

\[ V_{OUT} = V^+ - V_{DS} \]

\[ V_{OUT} = V_{DS} \]

SOURCE FOLLOWER

\[ \text{IN} \rightarrow \text{OUT} \]

\[ R_A \]

\[ R_B \]

CASCODE CURRENT SOURCES

\[ V^+ = +5V \]

\[ V^+ = +5V \]

\[ \text{ISOURCE} \]

\[ \text{ISET} \]

\[ \text{RSET} \]

Q1, Q2, Q3, Q4: N-Channel MOSFET

Q1, Q2, Q3, Q4: P-Channel MOSFET

\[ \text{ISOURCE} = \frac{V^+ - 2V_t}{R_{SET}} = \frac{3}{R_{SET}} \]
SOIC-8 PACKAGE DRAWING

8 Pin Plastic SOIC Package

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.35</td>
<td>0.053</td>
</tr>
<tr>
<td></td>
<td>1.75</td>
<td>0.069</td>
</tr>
<tr>
<td>A₁</td>
<td>0.10</td>
<td>0.004</td>
</tr>
<tr>
<td></td>
<td>0.25</td>
<td>0.010</td>
</tr>
<tr>
<td>b</td>
<td>0.35</td>
<td>0.014</td>
</tr>
<tr>
<td></td>
<td>0.45</td>
<td>0.018</td>
</tr>
<tr>
<td>C</td>
<td>0.18</td>
<td>0.007</td>
</tr>
<tr>
<td></td>
<td>0.25</td>
<td>0.010</td>
</tr>
<tr>
<td>D-8</td>
<td>4.69</td>
<td>0.185</td>
</tr>
<tr>
<td></td>
<td>5.00</td>
<td>0.196</td>
</tr>
<tr>
<td>E</td>
<td>3.50</td>
<td>0.140</td>
</tr>
<tr>
<td></td>
<td>4.05</td>
<td>0.160</td>
</tr>
<tr>
<td>e</td>
<td>1.27 BSC</td>
<td>0.050 BSC</td>
</tr>
<tr>
<td>H</td>
<td>5.70</td>
<td>0.224</td>
</tr>
<tr>
<td></td>
<td>6.30</td>
<td>0.248</td>
</tr>
<tr>
<td>L</td>
<td>0.60</td>
<td>0.024</td>
</tr>
<tr>
<td></td>
<td>0.937</td>
<td>0.037</td>
</tr>
<tr>
<td>Ø</td>
<td>0°</td>
<td>0°</td>
</tr>
<tr>
<td></td>
<td>8°</td>
<td>8°</td>
</tr>
<tr>
<td>S</td>
<td>0.25</td>
<td>0.010</td>
</tr>
<tr>
<td></td>
<td>0.50</td>
<td>0.020</td>
</tr>
</tbody>
</table>
PDIP-8 PACKAGE DRAWING

8 Pin Plastic DIP Package

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.81 5.08</td>
<td>0.105 0.200</td>
</tr>
<tr>
<td>A_1</td>
<td>0.38 1.27</td>
<td>0.015 0.050</td>
</tr>
<tr>
<td>A_2</td>
<td>1.27 2.03</td>
<td>0.050 0.080</td>
</tr>
<tr>
<td>b</td>
<td>0.89 1.65</td>
<td>0.035 0.065</td>
</tr>
<tr>
<td>b_1</td>
<td>0.38 0.51</td>
<td>0.015 0.020</td>
</tr>
<tr>
<td>c</td>
<td>0.20 0.30</td>
<td>0.008 0.012</td>
</tr>
<tr>
<td>D-8</td>
<td>9.40 11.68</td>
<td>0.370 0.460</td>
</tr>
<tr>
<td>E</td>
<td>5.59 7.11</td>
<td>0.220 0.280</td>
</tr>
<tr>
<td>E_1</td>
<td>7.62 8.26</td>
<td>0.300 0.325</td>
</tr>
<tr>
<td>e</td>
<td>2.29 2.79</td>
<td>0.090 0.110</td>
</tr>
<tr>
<td>e_1</td>
<td>7.37 7.87</td>
<td>0.290 0.310</td>
</tr>
<tr>
<td>L</td>
<td>2.79 3.81</td>
<td>0.110 0.150</td>
</tr>
<tr>
<td>S-8</td>
<td>1.02 2.03</td>
<td>0.040 0.080</td>
</tr>
<tr>
<td>ø</td>
<td>0° 15°</td>
<td>0° 15°</td>
</tr>
</tbody>
</table>