ADVANCED
LINEAR
DEVICES, INC.

ALD1721E

EPAD® MICROPOWER OPERATIONAL AMPLIFIER

KEY FEATURES

- **EPAD (Electrically Programmable Analog Device)**
- **User programmable V_{OS} trimmer**
- **Computer-assisted trimming**
- **Rail-to-rail input/output**
- **Compatible with standard EPAD Programmer**
- **High precision through in-system circuit precision trimming**
- **Reduces or eliminates V_{OS}, PSRR, CMRR and TCV_{OS} errors**
- **System level "calibration" capability**
- **Application Specific Programming mode**
- **In-System Programming mode**
- **Electrically programmable to compensate for external component tolerances**
- **Achieves 0.01pA input bias current and 35μV input offset voltage simultaneously**
- **Compatible with industry standard pinout**

GENERAL DESCRIPTION

The ALD1721E is a monolithic rail-to-rail precision CMOS operational amplifier with integrated user programmable EPAD (Electrically Programmable Analog Device) based offset voltage adjustment. The ALD1721E operational amplifier is a direct replacement of the ALD1701 operational amplifier, with the added feature of user-programmable offset voltage trimming resulting in significantly enhanced total system performance and user flexibility. EPAD technology is an exclusive ALD design which has been refined for analog applications where precision voltage trimming is necessary to achieve a desired performance. It utilizes CMOS FETs as in-circuit elements for trimming of offset voltage bias characteristics with the aid of a personal computer under software control. Once programmed, the set parameters are stored indefinitely within the device even after power-down. EPAD offers the circuit designer a convenient and cost-effective trimming solution for achieving the very highest amplifier/system performance.

The ALD1721E operational amplifier features rail-to-rail input and output voltage ranges, tolerance to over-voltage input spikes of 300mV beyond supply rails, capacitive loading up to 50pF, extremely low input currents of 0.01pA typical, high open loop voltage gain, useful bandwidth of 700KHz, slew rate of 0.7 V/μs, and low typical supply current of 120 uA.

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range		
0°C to +70°C	0°C to +70°C	-55°C to +125°C
8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package	8-Pin CERDIP Package
ALD1721ESAL	ALD1721EPAL	ALD1721EDA

* Contact factory for leaded (non-RoHS) or high temperature versions.

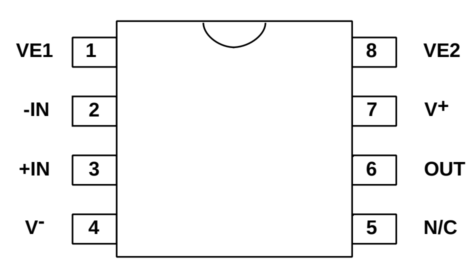
BENEFITS

- Eliminates manual and elaborate system trimming procedures
- Remote controlled automated trimming
- In-System Programming capability
- No external components
- No internal chopper clocking noise
- No chopper dynamic power dissipation
- Simple and cost effective
- Small package size
- Extremely small total functional volume size
- Low system implementation cost
- Micropower and Low Voltage

APPLICATIONS

- Sensor interface circuits
- Transducer biasing circuits
- Capacitive and charge integration circuits
- Biochemical probe interface
- Signal conditioning
- Portable instruments
- High source impedance electrode amplifiers
- Precision Sample and Hold amplifiers
- Precision current to voltage converter
- Error correction circuits
- Sensor compensation circuits
- Precision gain amplifiers
- Periodic In-system calibration
- System output level shifter

PIN CONFIGURATION



SAL, PAL, DA PACKAGES

FUNCTIONAL DESCRIPTION

The ALD1721E uses EPADs as in-circuit elements for trimming of offset voltage bias characteristics. Each ALD1721E has a pair of EPAD-based circuits connected such that one circuit is used to adjust V_{OS} in one direction and the other circuit is used to adjust V_{OS} in the other direction.

While each of the EPAD devices is a monotonically adjustable programmable device, the V_{OS} of the ALD1721E can be adjusted many times in both directions. Once programmed, the set V_{OS} levels are stored permanently, even when the device power is removed.

The ALD1721E provides the user with an operational amplifier that can be trimmed with user application-specific programming or in-system programming conditions. User application-specific circuit programming refers to the situation where the Total Input Offset Voltage of the ALD1721E can be trimmed with the actual intended operating conditions.

The ALD1721E is pre-programmed at the factory under standard operating conditions for minimum equivalent input offset voltage. It also has a guaranteed offset voltage program range, which is ideal for applications that require electrical offset voltage programming.

For example, an application circuit may have +6V and -2.5V power supplies, and the operational amplifier input is biased at +0.7V, and the average operating temperature is at 55°C. The circuit can be wired up to these conditions within an environmental chamber, and the ALD1721E can be inserted into a test socket connected to this circuit while it is being electrically trimmed. Any error in V_{OS} due to these bias conditions can be automatically zeroed out. The Total V_{OS} error is now limited only by the adjustable range and the stability of V_{OS}, and the input noise voltage of the operational amplifier. Therefore, this Total V_{OS} error now includes V_{OS} as V_{OS} is traditionally specified; plus the V_{OS} error contributions from PSRR, CMRR, TCV_{OS}, and noise. Typically this total V_{OS} error term (V_{OST}) is approximately ±35μV for the ALD1721E.

The V_{OS} contribution due to PSRR, CMRR, TCV_{OS} and external components can be large for operational amplifiers without trimming. Therefore the ALD1721E with EPAD trimming is able to provide much improved system performance by reducing these other sources of error to provide significantly reduced V_{OST}.

In-System Programming refers to the condition where the EPAD adjustment is made after the ALD1721E has been inserted into a circuit board. In this case, the circuit design must provide for the ALD1721E to operate in normal mode and in programming mode. One of the benefits of in-system programming is that not only is the ALD1721E offset voltage from operating bias conditions accounted for, any residual errors introduced by other circuit components, such as resistor or sensor induced voltage errors, can also be corrected. In this way, the "in-system" circuit output can be adjusted to a desired level eliminating other trimming components.

USER PROGRAMMABLE Vos FEATURE

Each ALD1721E has two pins named VE1 and VE2 which are internally connected to an internal offset bias circuit. VE1/VE2 have initial typical values of 1.2 /1.7 Volt. The voltage on these pins can be programmed using the ALD E100 EPAD Programmer and the appropriate Adapter Module. The useful programming range of VE1 and VE2 is 1.2 Volt to 3.0 Volts. VE1 and VE2 pins are programming pins, used during programming mode. The Programming pin is used during electrical programming to inject charge into the internal EPADs. Increases of VE1 decrease the offset voltage while increases of VE2 increase the offset voltage of the operational amplifier. The injected charge is permanently stored and determines the offset voltage of the operational amplifier. After programming, VE1 and VE2 terminals must be left open to settle on a voltage determined by internal bias currents.

During programming, the voltages on VE1 or VE2 are increased incrementally to set the offset voltage of the operational amplifier to the desired V_{OS}. Note that desired V_{OS} can be any value within the offset voltage programmable ranges, and can be either zero, a positive value or a negative value. This V_{OS} value can also be reprogrammed to a different value at a later time, provided that the useful VE1 or VE2 programming voltage range has not been exceeded. VE1 or VE2 pins can also serve as capacitively coupled input pins.

Internally, VE1 and VE2 are programmed and connected differentially. Temperature drift effects between the two internal offset bias circuits cancel each other and introduce less net temperature drift coefficient change than offset voltage trimming techniques such as offset adjustment with an external trimmer potentiometer.

While programming, V+, VE1 and VE2 pins may be alternately pulsed with 12V (approximately) pulses generated by the EPAD Programmer. In-system programming requires the ALD1721E application circuit to accommodate these programming pulses. This can be accomplished by adding resistors at certain appropriate circuit nodes. For more information, see Application Note AN1700.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V^+		13.2V
Differential input voltage range		-0.3V to V^+ +0.3V
Power dissipation		600 mW
Operating temperature range	SAL, PAL packages	0°C to +70°C
	DA package	-55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature, 10 seconds		+260°C

OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C V_S = ±2.5V unless otherwise specified

Parameter	Symbol	1721E Min	1721E Typ	1721E Max	Unit	Test Conditions
Supply Voltage	V_S V^+	±1.0 2.0		±5.0 10.0	V V	 Single Supply
Initial Input Offset Voltage[1]	$V_{OS\,i}$		35	90	µV	R_S ≤ 100KΩ
Offset Voltage Program Range [2]	ΔV_{OS}	±10	±15		mV	
Programmed Input Offset Voltage Error [3]	V_{OS}		50	90	µV	At user specified target offset voltage
Total Input Offset Voltage [4]	V_{OST}		50	90	µV	At user specified target offset voltage
Input Offset Current [5]	I_{OS}		0.01	10 240	pA pA	T_A = 25°C 0°C ≤ T_A ≤ +70°C
Input Bias Current [5]	I_B		0.01	10 240	pA pA	T_A = 25°C 0°C ≤ T_A ≤ +70°C
Input Voltage Range [6]	V_{IR}	-0.3 -2.8		5.3 +2.8	V V	V^+ = +5V V_S = ±2.5V
Input Resistance	R_{IN}		10^{14}		Ω	
Input Offset Voltage Drift [7]	TCV_{OS}		5		µV/°C	R_S ≤ 100KΩ
Initial Power Supply Rejection Ratio [8]	$PSRR_i$		80		dB	R_S ≤ 100KΩ
Initial Common Mode Rejection Ratio [8]	$CMRR_i$		83		dB	R_S ≤ 100KΩ
Large Signal Voltage Gain	A_V	32 20	100		V/mV V/mV	R_L =100KΩ 0°C ≤ T_A ≤ +70°C
Output Voltage Range	V_O low V_O high	 4.99	0.001 4.999	0.01	V V	R_L =1MΩ V^+ = 5V 0°C ≤ T_A ≤ +70°C
	V_O low V_O high	 2.40	-2.48 2.48	-2.40	V V	R_L =100KΩ 0°C ≤ T_A ≤ +70°C
Output Short Circuit Current	I_{SC}		1		mA	

* NOTES 1 through 9, see "Definitions and Design Notes" on page 6.

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

T_A = 25°C V_S = ±2.5V unless otherwise specified

Parameter	Symbol	1721E Min	Typ	Max	Unit	Test Conditions
Supply Current	I_S		120	200	µA	V_{IN} = 0V No Load
Power Dissipation	P_D		0.6	1.00	mW	V_S = ±2.5V
Input Capacitance	C_{IN}		1		pF	
Maximum Load Capacitance	C_L		50		pF	
Equivalent Input Noise Voltage	e_n		55		nV/√Hz	f = 1KHz
Equivalent Input Current Noise	i_n		0.6		fA/√Hz	f =10Hz
Bandwidth	B_W	400	700		KHz	
Slew Rate	S_R	0.3	0.7		V/µs	A_V = +1 R_L = 10KΩ
Rise time	t_r		0.2		µs	R_L = 10KΩ
Overshoot Factor			20		%	R_L = 100KΩ, C_L = 50pF
Settling Time	t_s		10		µs	0.1% A_V = 1,R_L=100KΩ C_L = 50pF

T_A = 25°C V_S = ±2.5V unless otherwise specified

Parameter	Symbol	1721E Min	Typ	Max	Unit	Test Conditions
Average Long Term Input Offset Voltage Stability [9]	$\frac{\Delta V_{OS}}{\Delta time}$		0.02		µV/ 1000 hrs	
Initial VE Voltage	$VE1_i$, $VE2_i$		1.2		V	
Programmable VE Range	ΔVE1, ΔVE2	1.5	2.5		V	
Programmed VE Voltage Error	e(VE1-VE2)		0.1		%	
VE Pin Leakage Current	i_{eb}		-5		µA	

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

V_S = ±2.5V -55°C ≤ T_A ≤ +125°C unless otherwise specified

Parameter	Symbol	1721E Min	1721E Typ	1721E Max	Unit	Test Conditions
Initial Input offset Voltage	$V_{OS\,i}$		0.5		mV	R_S ≤ 100KΩ
Input Offset Current	I_{OS}			2.0	nA	
Input Bias Current	I_B			2.0	nA	
Initial Power Supply Rejection Ratio [8]	$PSRR_i$		75		dB	R_S ≤ 100KΩ
Initial Common Mode Rejection Ratio [8]	$CMRR_i$		83		dB	R_S ≤ 100KΩ
Large Signal Voltage Gain	A_V	15	50		V/mV	R_L = 100KΩ
Output Voltage Range	V_O low V_O high	 2.35	-2.47 2.45	-2.40	V V	 R_L = 100KΩ

T_A = 25°C V_S = ±5.0V unless otherwise specified

Parameter	Symbol	1721E Min	1721E Typ	1721E Max	Unit	Test Conditions
Initial Power Supply Rejection Ratio [8]	$PSRR_i$		83		dB	R_S ≤ 100KΩ
Initial Common Mode Rejection Ratio [8]	$CMRR_i$		83		dB	R_S ≤ 100KΩ
Large Signal Voltage Gain	A_V		250		V/mV	R_L = 100KΩ
Output Voltage Range	V_O low V_O high	 4.90	-4.98 4.98	-4.90	V	R_L = 100KΩ
Bandwidth	B_W		1.0		MHz	
Slew Rate	S_R		1.0		V/µs	A_V = +1, C_L = 50pF

DEFINITIONS AND DESIGN NOTES:

1. Initial Input Offset Voltage is the initial offset voltage of the ALD1721E operational amplifier when shipped from the factory. The device has been pre-programmed and tested for programmability.

2. Offset Voltage Program Range is the range of adjustment of user specified target offset voltage. This is typically an adjustment in either the positive or the negative direction of the input offset voltage from an initial input offset voltage. The input offset programming pins, VE1 or VE2, change the input offset voltage in the negative or positive direction, respectively. User specified target offset voltage can be any offset voltage within this programming range.

3. Programmed Input Offset Voltage Error is the final offset voltage error after programming when the Input Offset Voltage is at target Offset Voltage. This parameter is sample tested.

4. Total Input Offset Voltage is the same as Programmed Input Offset Voltage, corrected for system offset voltage error. Usually this is an all inclusive system offset voltage, which also includes offset voltage contributions from input offset voltage, PSRR, CMRR, TCV_{OS} and noise. It can also include errors introduced by external components, at a system level. Programmed Input Offset Voltage and Total Input Offset Voltage is not necessarily zero offset voltage, but an offset voltage set to compensate for other system errors as well. This parameter is sample tested.

5. The Input Offset and Bias Currents are essentially input protection diode reverse bias leakage currents. This low input bias current assures that the analog signal from the source will not be distorted by it. For applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

6. Input Voltage Range is determined by two parallel complementary input stages that are summed internally, each stage having a separate input offset voltage. While Total Input Offset Voltage can be trimmed to a desired target value, it is essential to note that this trimming occurs at only one user selected input bias voltage. Depending on the selected input bias voltage relative to the power supply voltages, offset voltage trimming may affect one or both input stages. For the ALD1721E, the switching point between the two stages occur at approximately 1.5V below positive supply voltage.

7. Input Offset Voltage Drift is the average change in Total Input Offset Voltage as a function of ambient temperature. This parameter is sample tested.

8. Initial PSRR and initial CMRR specifications are provided as reference information. After programming, error contribution to the offset voltage from PSRR and CMRR is set to zero under the specific power supply and common mode conditions, and becomes part of the Programmed Input Offset Voltage Error.

9. Average Long Term Input Offset Voltage Stability is based on input offset voltage shift through operating life test at 125°C extrapolated to T_A = 25 °C, assuming activation energy of 1.0eV. This parameter is sample tested.

ADDITIONAL DESIGN NOTES:

A. The ALD1721E is internally compensated for unity gain stability using a novel scheme which produces a single pole role off in the gain characteristics while providing more than 70 degrees of phase margin at unity gain frequency. A unity gain buffer using the ALD1721E will typically drive 50pF of external load capacitance.

B. The ALD1721E has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail-to-rail input common mode voltage range. The switching point between the two differential stages is 1.5V below positive supply voltage. For applications such as inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), the common mode voltage does not make excursions below this switching point. However, this switching does take place if the operational amplifier is connected as a rail-to-rail unity gain buffer and the design must allow for input offset voltage variations.

C. The output stage consists of class AB complementary output drivers. The oscillation resistant feature, combined with the rail-to-rail input and output feature, makes the ALD1721E an effective analog signal buffer for high source impedance sensors, transducers, and other circuit networks.

D. The ALD1721E has static discharge protection. Care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. The user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages not to exceed 0.3V of the power supply voltage levels.

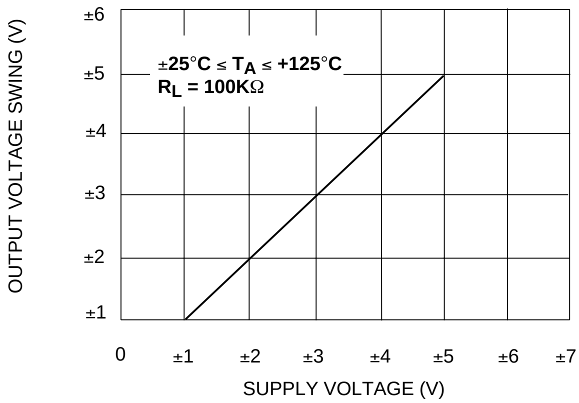
E. VE1 and VE2 are high impedance terminals, as the internal bias currents are set very low to a few microamperes to conserve power. For some applications, these terminals may need to be shielded from external coupling sources. For example, digital signals running nearby may cause unwanted offset voltage fluctuations. Care during the printed circuit board layout to place ground traces around these pins and to isolate them from digital lines will generally eliminate such coupling effects. In addition, optional decoupling capacitors of 1000pF or greater value can be added to VE1 and VE2 terminals.

F. The ALD1721E is designed for use in low voltage, micropower circuits. The maximum operating voltage during normal operation should remain below 10 Volts at all times. Care should be taken to insure that the application in which the device is used do not experience any positive or negative transient voltages that will cause any of the terminal voltages to exceed this limit.

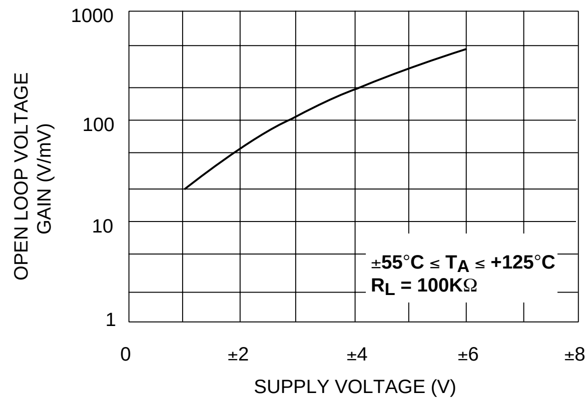
G. All inputs or unused pins except VE1 and VE2 pins should be connected to a supply voltage such as Ground so that they do not become floating pins, since input impedance at these pins is very high. If any of these pins are left undefined, they may cause unwanted oscillation or intermittent excessive current drain. As these devices are built with CMOS technology, normal operating and storage temperature limits, ESD and latchup handling precautions pertaining to CMOS device handling should be observed.

TYPICAL PERFORMANCE CHARACTERISTICS

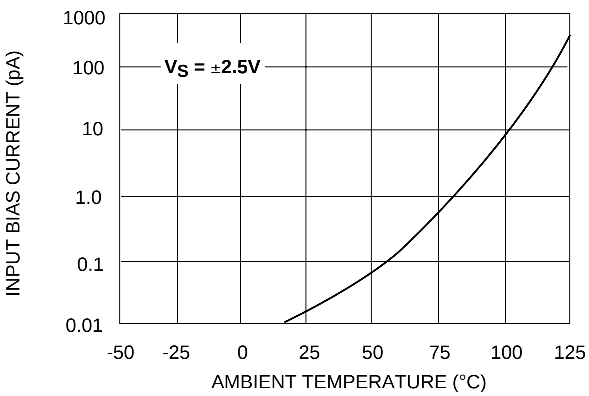
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



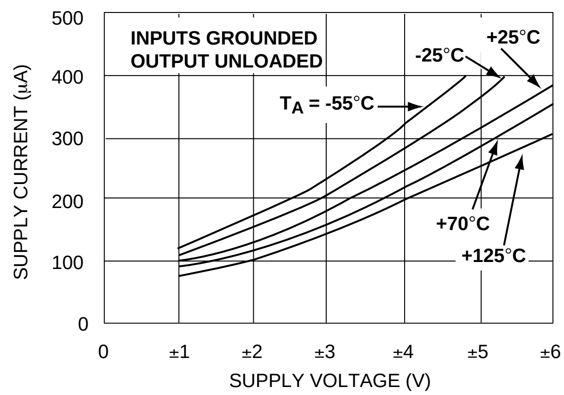
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE



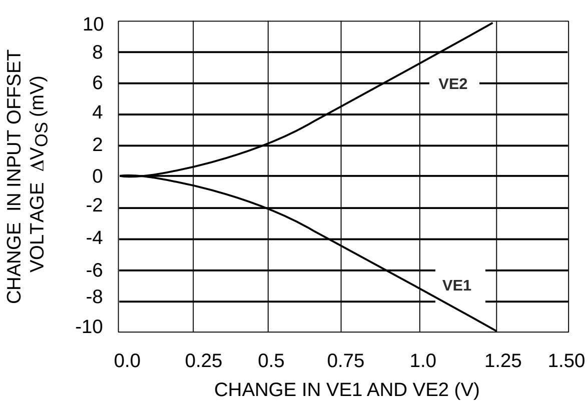
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



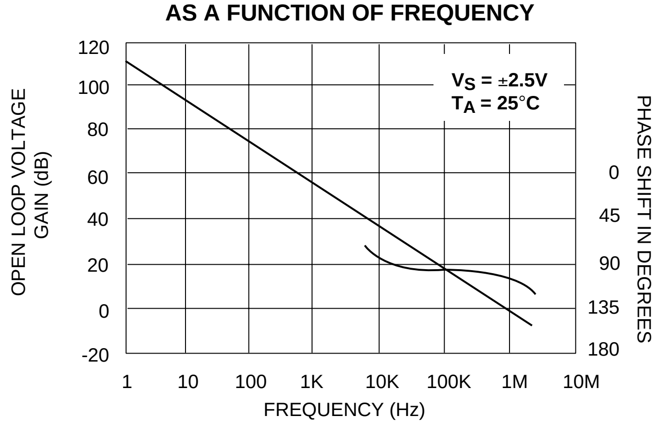
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



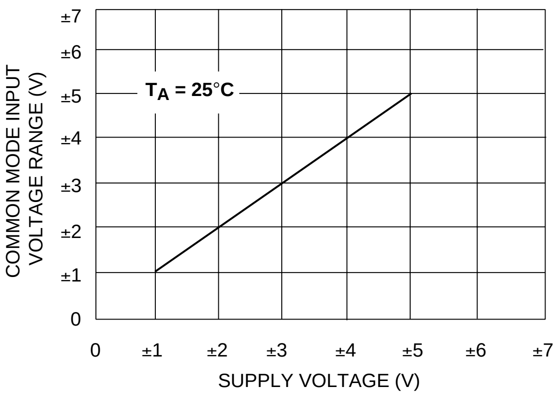
ADJUSTMENT IN INPUT OFFSET VOLTAGE AS A FUNCTION OF CHANGE IN VE1 AND VE2



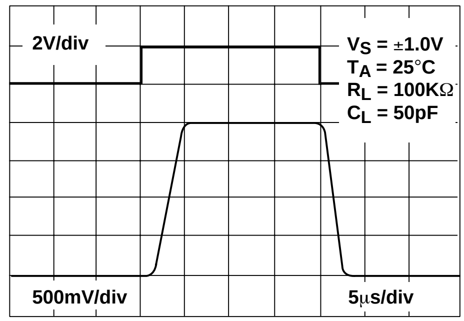
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



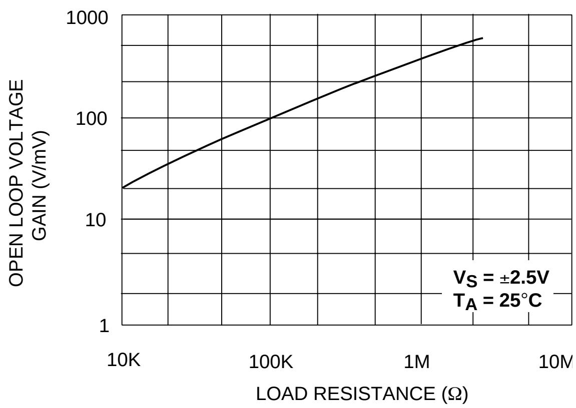
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



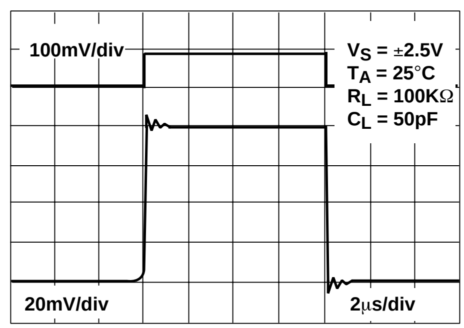
LARGE - SIGNAL TRANSIENT RESPONSE



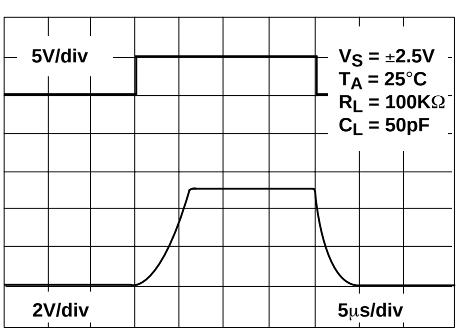
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



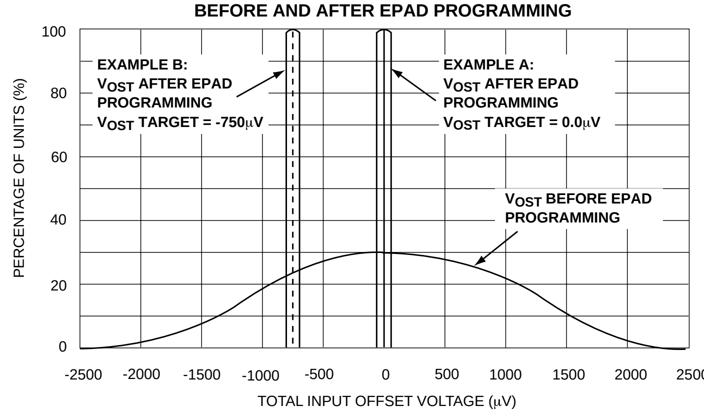
SMALL - SIGNAL TRANSIENT RESPONSE



LARGE - SIGNAL TRANSIENT RESPONSE

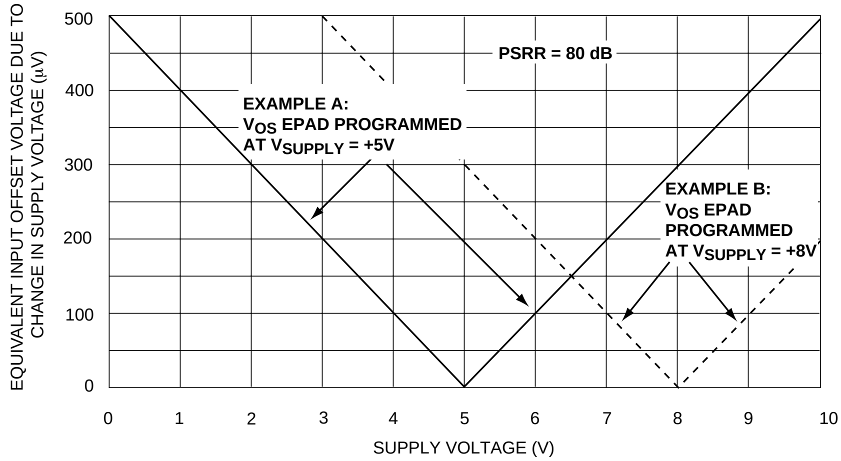


DISTRIBUTION OF TOTAL INPUT OFFSET VOLTAGE BEFORE AND AFTER EPAD PROGRAMMING

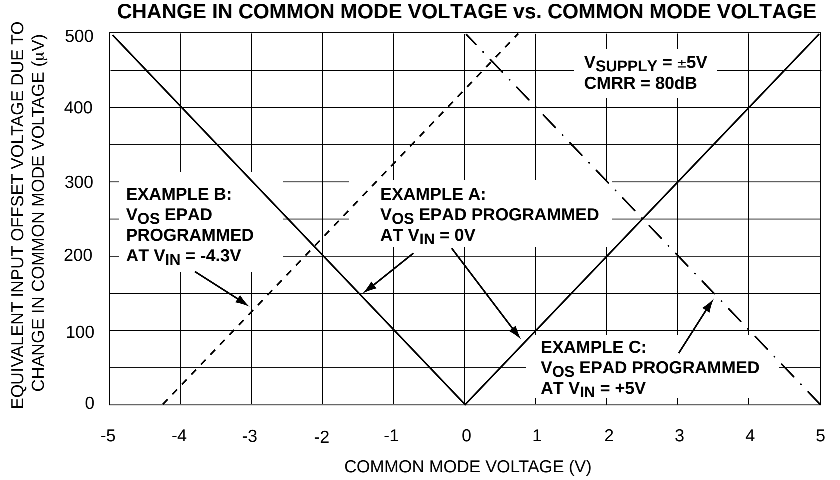


TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

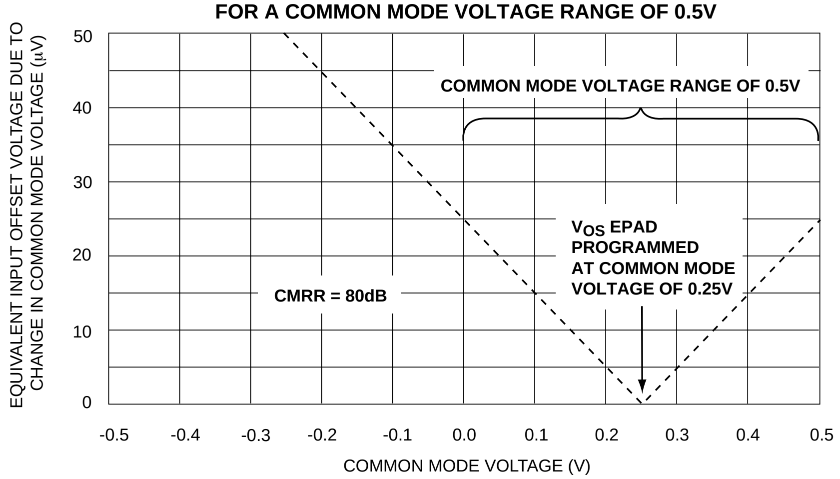
TWO EXAMPLES OF EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN SUPPLY VOLTAGE vs. SUPPLY VOLTAGE



THREE EXAMPLES OF EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN COMMON MODE VOLTAGE vs. COMMON MODE VOLTAGE

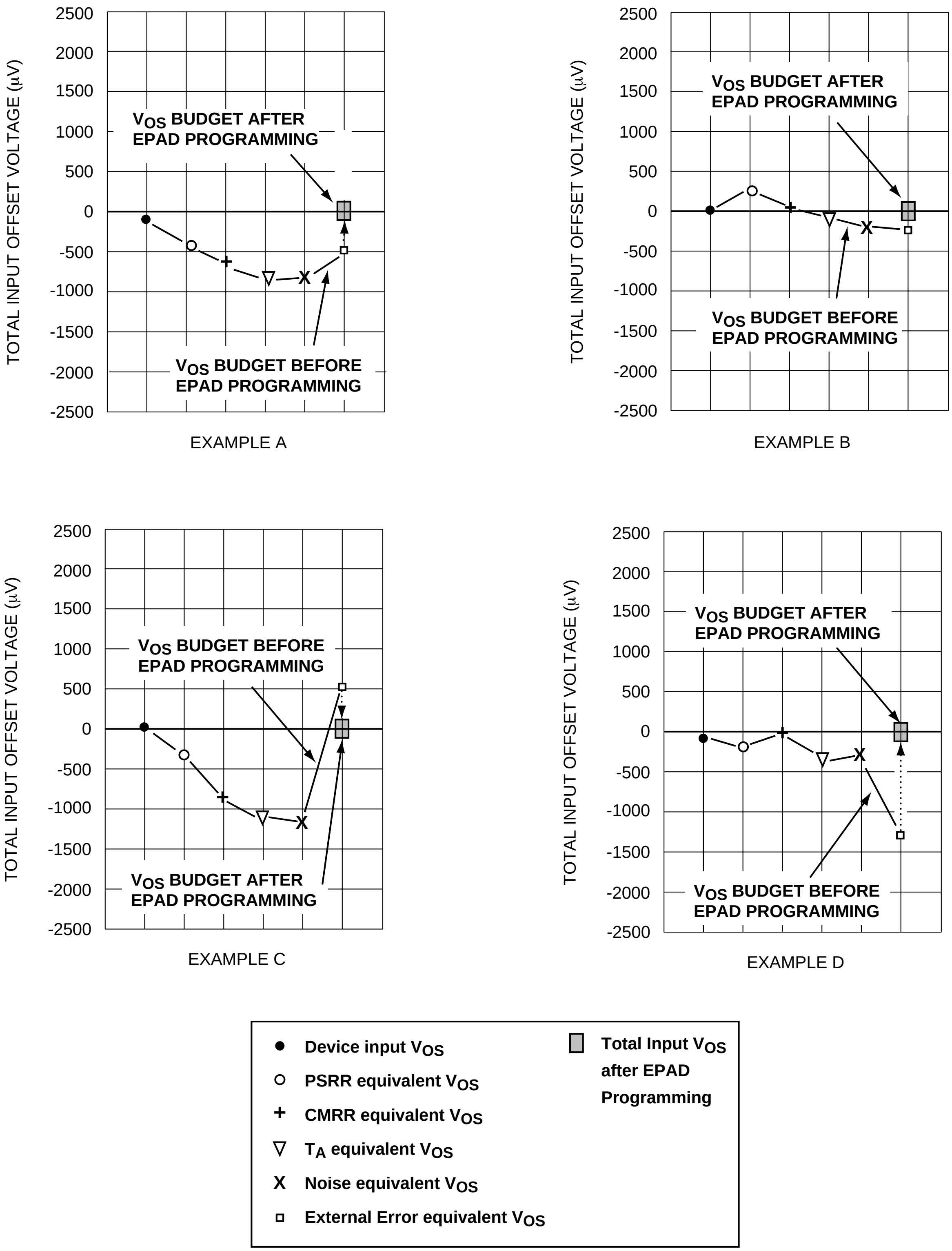


EXAMPLE OF MINIMIZING EQUIVALENT INPUT OFFSET VOLTAGE FOR A COMMON MODE VOLTAGE RANGE OF 0.5V



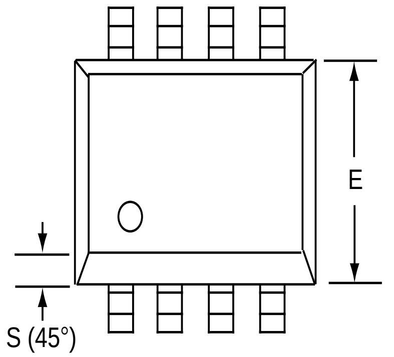
APPLICATION SPECIFIC / IN-SYSTEM PROGRAMMING

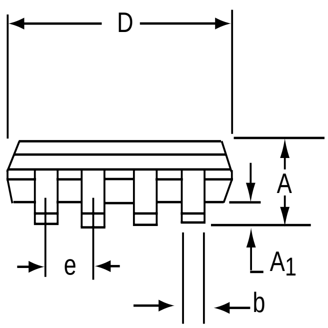
Examples of applications where accumulated total input offset voltage from various contributing sources is minimized under different sets of user-specified operating conditions

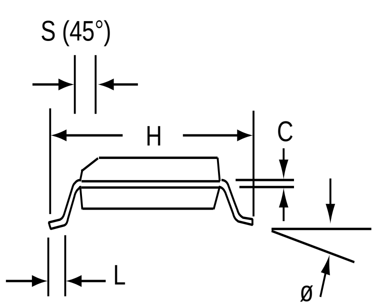


SOIC-8 PACKAGE DRAWING

8 Pin Plastic SOIC Package



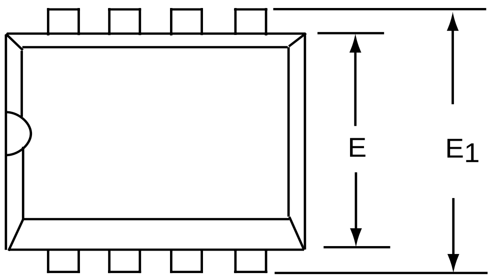


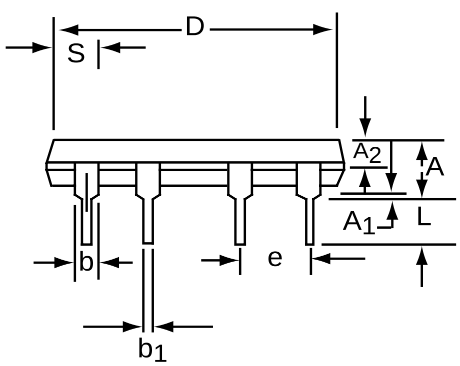


Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

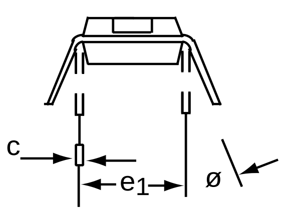
PDIP-8 PACKAGE DRAWING

8 Pin Plastic DIP Package



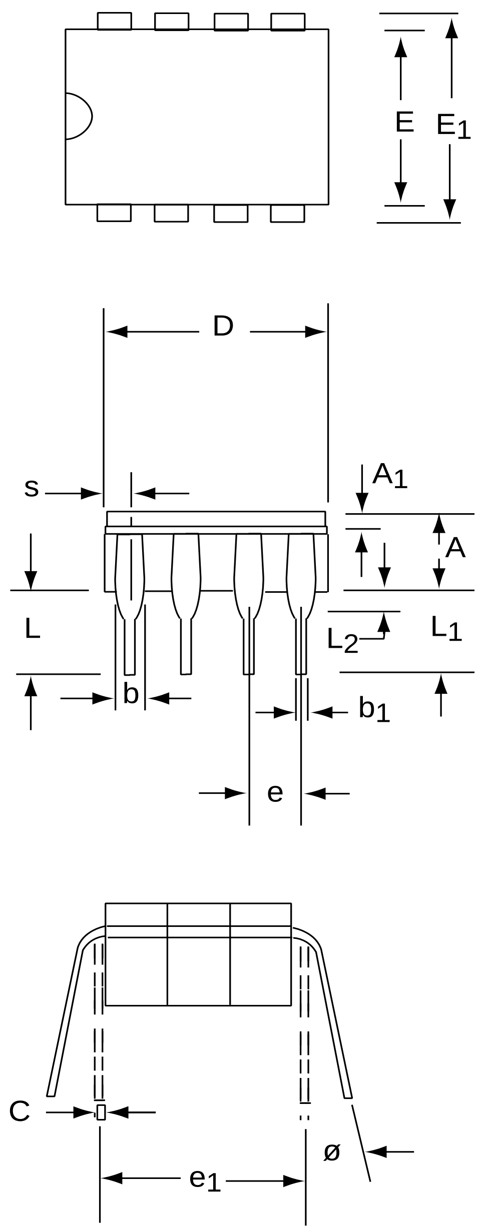


Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.40	11.68	0.370	0.460
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°



CERDIP-8 PACKAGE DRAWING

8 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A_1	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b_1	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-8	--	10.29	--	0.405
E	5.59	7.87	0.220	0.310
E_1	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	--	0.125	--
L_2	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°