GENERAL DESCRIPTION

The ALD212900A/ALD212900 precision N-Channel EPAD® MOSFET array is precision matched at the factory using ALD’s proven EPAD® CMOS technology. These dual monolithic devices are enhanced additions to the ALD110900A/ALD110900 EPAD® MOSFET Family, with increased forward transconductance and output conductance, particularly at very low supply voltages.

Intended for low voltage, low power small signal applications, the ALD212900A/ALD212900 features Zero-Threshold™ voltage, which enables circuit designs with input/output signals referenced to GND at enhanced operating voltage ranges. With these devices, a circuit with multiple cascading stages can be built to operate at extremely low supply/bias voltage levels. For example, a nanopower input amplifier stage operating at less than 0.2V supply voltage has been successfully built with these devices.

ALD212900A EPAD MOSFETs feature exceptional matched pair device electrical characteristics of Gate Threshold Voltage $V_{GS(th)}$ set precisely at 0.00V ±0.01V, $I_D = +200\mu A$ @ $V_{DS} = 0.1\text{V}$, with a typical offset voltage of only ±0.001V (1mV). Built on a single monolithic chip, they also exhibit excellent temperature tracking characteristics. These precision devices are versatile as design components for a broad range of analog small signal applications such as basic building blocks for current mirrors, matching circuits, current sources, differential amplifier input stages, transmission gates, and multiplexers. They also excel in limited operating voltage applications, such as very low level voltage-clamps and nano-power normally-on circuits.

In addition to precision matched-pair electrical characteristics, each individual EPAD MOSFET also exhibits well controlled manufacturing characteristics, enabling the user to depend on tight design limits from different production batches. These devices are built for minimum voltage offset and differential thermal response, and they can be used for switching and amplifying applications in +0.1V to +10V (+0.05V to ±5V) powered systems where low input bias current, low input capacitance, and fast switching speed are desired. At $V_{GS} > 0.00\text{V}$, the device exhibits enhancement mode characteristics whereas at $V_{GS} < 0.00\text{V}$ the device operates in the subthreshold voltage region and exhibits conventional depletion mode characteristics, with well controlled turn-off and sub-threshold levels that operate the same as standard enhancement mode MOSFETs.

The ALD212900A/ALD212900 features high input impedance (2.5 x 10^10 Ω) and high DC current gain (>10^8). A sample calculation of the DC current gain at a drain output current of 30mA and input current of 300pA at 25°C is 30mA/300pA = 100,000,000, which translates into a dynamic operating current range of about eight orders of magnitude. A series of four graphs titled “Forward Transfer Characteristics”, with the 2\text{nd} and 3\text{rd} sub-titled “expanded (subthreshold)”, and the 4\text{th} sub-titled “low voltage”, illustrates the wide dynamic operating range of these devices.

Generally it is recommended that the $V_+$ pin be connected to the most positive voltage and the $V_-$ and IC (internally-connected) pins to the most negative voltage in the system. All other pins must have voltages within these voltage limits at all times. Standard ESD protection facilities and handling procedures for static sensitive devices are highly recommended when using these devices.

ORDERING INFORMATION (“L” suffix denotes lead-free (RoHS))

<table>
<thead>
<tr>
<th>Operating Temperature Range *</th>
<th>0°C to +70°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Pin SOIC Package</td>
<td>8-Pin Plastic Dip Package</td>
</tr>
<tr>
<td>ALD212900ASAL</td>
<td>ALD212900APAL</td>
</tr>
<tr>
<td>ALD212900SAL</td>
<td>ALD212900PAL</td>
</tr>
</tbody>
</table>

*Contact factory for industrial temp. range or user-specified threshold voltage values.

FEATURES & BENEFITS

- Zero Threshold™ $V_{GS(th)} = 0.00V ±0.01V$
- $V_{OS}$ (two $V_{GS(th)}$ match) to 2mV/10mV max.
- Sub-threshold voltage (nano-power) operation
- < 100mV min. operating voltage
- < 1nA min. operating current
- < 1nW min. operating power
- > 100,000,000:1 operating current ranges
- High transconductance and output conductance
- Low $R_{DS(ON)}$ of 14Ω
- Output current >50mA
- Matched and tracked tempco
- Tight lot-to-lot parametric control
- Positive, zero, and negative $V_{GS(th)}$ tempco
- Low input capacitance and leakage currents

APPLICATIONS

- Low overhead current mirrors and current sources
- Zero Power Normally-On circuits
- Energy harvesting circuits
- Very low voltage analog and digital circuits
- Zero power fail-safe circuits
- Backup battery circuits & power failure detector
- Extremely low level voltage-clamps
- Extremely low level zero-crossing detector
- Matched source followers and buffers
- Precision current mirrors and current sources
- Matched capacitive probes and sensor interfaces
- Charge detectors and charge integrators
- High gain differential amplifier input stage
- Matched peak-detectors and level-shifters
- Multiple Channel Sample-and-Hold switches
- Precision Current multipliers
- Discrete matched analog switches/multiplexers
- Nanopower discrete voltage comparators

PIN CONFIGURATION

- $IC^*$ pins are internally connected, connect to $V_-$

*SAL, PAL PACKAGES

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### OPERATING ELECTRICAL CHARACTERISTICS

\( V^+ = +5V \quad V^- = GND \quad TA = 25^\circ C \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>ALD212900A</th>
<th></th>
<th>ALD212900</th>
<th></th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Threshold Voltage</td>
<td>( V_{GS(th)} )</td>
<td>-0.02</td>
<td>0.00</td>
<td>0.02</td>
<td>-0.02</td>
<td>0.00</td>
<td>0.02 V ( I_{DS} = 20\mu A, V_{DS} = 0.1V )</td>
</tr>
<tr>
<td>Offset Voltage</td>
<td>( V_{OS} )</td>
<td>1.8</td>
<td>3.8</td>
<td>2</td>
<td>10</td>
<td>mV/V</td>
<td>( V_{GS(th)}M1 - V_{GS(th)}M2 )</td>
</tr>
<tr>
<td>Offset Voltage Tempco</td>
<td>( TCV_{OS} )</td>
<td>5</td>
<td>5</td>
<td></td>
<td></td>
<td>( \mu V/^\circ C ) ( V_{DS1} = V_{DS2} )</td>
<td></td>
</tr>
<tr>
<td>Gate Threshold Voltage Tempco</td>
<td>( TCV_{GS(th)} )</td>
<td>-1.7</td>
<td>0.0</td>
<td>+0.6</td>
<td>-1.7</td>
<td>0.0</td>
<td>+1.6 mV/V/(^\circ C ) ( I_{D} = 20\mu A, V_{DS} = 0.1V ) ( I_{D} = 760\mu A, V_{DS} = 0.1V ) ( I_{D} = 1.5mA, V_{DS} = 0.1V )</td>
</tr>
<tr>
<td>On Drain Current</td>
<td>( I_{DS(ON)} )</td>
<td>79</td>
<td>79</td>
<td></td>
<td>85</td>
<td>( mA )</td>
<td>( V_{GS} = +3.0V, V_{DS} = +3V )</td>
</tr>
<tr>
<td>Forward Transconductance</td>
<td>( G_{FS} )</td>
<td>38</td>
<td>38</td>
<td></td>
<td></td>
<td>mmho</td>
<td>( V_{GS} = +3.0V ) ( V_{DS} = +3.0V )</td>
</tr>
<tr>
<td>Transconductance Mismatch</td>
<td>( \Delta G_{FS} )</td>
<td>1.8</td>
<td>1.8</td>
<td></td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Output Conductance</td>
<td>( G_{OS} )</td>
<td>2.3</td>
<td>2.3</td>
<td></td>
<td></td>
<td>mmho</td>
<td>( V_{GS} = +3.0V ) ( V_{DS} = +3.0V )</td>
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<tr>
<td>Drain Source On Resistance</td>
<td>( R_{DS(ON)} )</td>
<td>14</td>
<td>14</td>
<td></td>
<td></td>
<td>( \Omega )</td>
<td>( V_{GS} = +5.0V ) ( V_{DS} = +0.1V )</td>
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<tr>
<td>Drain Source On Resistance</td>
<td>( R_{DS(ON)} )</td>
<td>5</td>
<td>1.18</td>
<td></td>
<td>5</td>
<td>1.18</td>
<td>( \kappa \Omega ) ( V_{GS} = +0.0V, V_{DS} = +0.1V ) ( V_{GS} = +0.1V, V_{DS} = +0.1V )</td>
</tr>
<tr>
<td>Drain Source On Resistance Tolerance</td>
<td>( \Delta R_{DS(ON)} )</td>
<td>1.8</td>
<td>1.8</td>
<td></td>
<td></td>
<td>%</td>
<td>( V_{GS} = +5.0V ) ( V_{DS} = +0.1V )</td>
</tr>
<tr>
<td>Drain Source On Resistance Mismatch</td>
<td>( \Delta R_{DS(ON)} )</td>
<td>0.6</td>
<td>0.6</td>
<td></td>
<td></td>
<td>%</td>
<td></td>
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<tr>
<td>Drain Source Breakdown Voltage</td>
<td>( B_{VDSX} )</td>
<td>10</td>
<td>10</td>
<td></td>
<td></td>
<td>V</td>
<td>( V^- = V_{GS} = -1.0V ) ( I_{DS} = 10\mu A )</td>
</tr>
<tr>
<td>Drain Source Leakage Current(^1)</td>
<td>( I_{DS(OFF)} )</td>
<td>10</td>
<td>400</td>
<td>4</td>
<td>10</td>
<td>400</td>
<td>( pA ) ( V_{GS} = +1.0V, V_{DS} = +5V ) ( V^- = +5V ) ( T_A = 125^\circ C )</td>
</tr>
<tr>
<td>Gate Leakage Current(^1)</td>
<td>( I_{GSS} )</td>
<td>5</td>
<td>200</td>
<td>1</td>
<td>5</td>
<td>200</td>
<td>( pA ) ( V_{GS} = +5V, V_{DS} = 0V ) ( T_A = 125^\circ C )</td>
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<tr>
<td>Input Capacitance</td>
<td>( C_{ISS} )</td>
<td>30</td>
<td>30</td>
<td></td>
<td></td>
<td>( pF )</td>
<td></td>
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<tr>
<td>Transfer Reverse Capacitance</td>
<td>( C_{RSS} )</td>
<td>2</td>
<td>2</td>
<td></td>
<td></td>
<td>( pF )</td>
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<tr>
<td>Turn-on Delay Time</td>
<td>( t_{on} )</td>
<td>10</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
<td>( V^+ = 5V, RL = 5K\Omega )</td>
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<tr>
<td>Turn-off Delay Time</td>
<td>( t_{off} )</td>
<td>10</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
<td>( V^+ = 5V, RL = 5K\Omega )</td>
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<tr>
<td>Crosstalk</td>
<td></td>
<td>60</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
<td>( f = 100KHz )</td>
</tr>
</tbody>
</table>

Notes: \(^1\) Consists of junction leakage currents
PERFORMANCE CHARACTERISTICS OF EPAD® PRECISION MATCHED PAIR MOSFET FAMILY

The ALD2148xx/ALD2169xx (quad/dual) features Depletion Mode MOSFETs, which are normally-on devices at zero applied gate voltage. The \( V_{GS(th)} \) is set at a negative voltage level \((V < V_{GS} < V_{D})\) at which the EPAD MOSFET turns off. Without a supply voltage and/or with \( V_{GS} = 0.00V \) = Ground, the EPAD MOSFET device is already turned on and exhibits a defined and controlled on-resistance \( R_{DS(on)} \). An EPAD MOSFET may be turned off when a negative voltage is applied to \( V \)-pin and \( V_{GS} \) set more negative than its \( V_{GS(th)} \). These Depletion Mode EPAD MOSFETs are different from most other depletion mode MOSFETs and JFETs in that they do not exhibit high gate leakage currents and channel/junction leakage currents, while they stay controlled, modulated and turned off at precise voltages. The same MOSFET device equations as those for enhancement mode devices apply.

KEY APPLICATION ENVIRONMENTS

EPAD MOSFETs are ideal for circuits requiring low \( V_{OS} \) and low operating currents with tracked differential thermal responses. They feature low input bias currents (less than 200pA max.), low input capacitance and fast switching speed. These and other operating characteristics offer unique solutions in one or more of the following operating environments:

- Low supply voltage: 0.1V to 10V (\( \pm 0.05V \) to \( \pm 5V \))
- Ultra low supply voltage: \( < 210mV \) to \( \pm 0.1V \)
- Nanopower operation: voltage x current = nW or \( \mu \)W
- Precision \( V_{OS} \) characteristics
- Matching and tracking of multiple MOSFETs
- Matching across multiple packages

ELECTRICAL CHARACTERISTICS

The turn-on and turn-off electrical characteristics of the EPAD MOSFET products are shown in the \( I_{DS(on)} \) vs. \( V_{DS(on)} \) and \( I_{DS(on)} \) vs. \( V_{GDS(on)} \) graphs. Each graph shows \( I_{DS(on)} \) versus \( V_{DS(on)} \) and \( V_{GDS(on)} \) characteristics as a function of \( V_{GS} \) in a different operating region under different bias conditions, while \( I_{DS(on)} \) at a given gate input voltage is controlled and predictable. A series of four graphs titled “Forward Transfer Characteristics”, with the 2nd and 3rd sub-titled “expanded (subthreshold)” and “further expanded (subthreshold)”, and the 4th sub-titled “low voltage”, illustrates the wide dynamic operating range of these devices.

Classic MOSFET equations for an N-channel MOSFET also apply to EPAD MOSFETs.

The drain current in the linear region \((V_{DS(on)} < V_{GS} - V_{GS(th)}\)) is given by:

\[
I_{DS(on)} = u \cdot COX \cdot W/L \cdot (V_{GS} - V_{GS(th)} - V_{DS/2}) \cdot V_{DS(on)}
\]

where:

- \( u \) = Mobility
- \( COX \) = Capacitance / unit area of Gate electrode
- \( V_{GS} \) = Gate to Source Voltage
- \( V_{GS(th)} \) = Gate Threshold (Turn-on) Voltage
- \( V_{DS(on)} \) = Drain to Source On Voltage
- \( W \) = Channel width
- \( L \) = Channel length

In this region of operation the \( V_{DS(on)} \) value is proportional to the \( V_{DS(on)} \) value and the device can be used as a gate-voltage controlled resistor.

For higher values of \( V_{DS(on)} \) where \( V_{DS(on)} \geq V_{GS} - V_{GS(th)} \), the saturation current \( I_{DS(on)} \) is now given by (approx.):

\[
I_{DS(on)} = u \cdot COX \cdot W/L \cdot (V_{GS} - V_{GS(th)})^2
\]
SUB-THRESHOLD REGION OF OPERATION

The gate threshold (turn-on) voltage $V_{G(S)}(th)$ of the EPAD MOSFET is a voltage below which the MOSFET conduction channel rapidly turns off. For analog designs, this gate threshold voltage directly affects the operating signal voltage range and the operating bias current levels.

At a voltage below $V_{G(S)}(th)$, an EPAD MOSFET exhibits a turn-off characteristic in an operating region called the subthreshold region. This is when the EPAD MOSFET conduction channel rapidly turns off as a function of decreasing applied gate voltage. The conduction channel, induced by the gate voltage on the gate electrode, decreases exponentially and causes the drain current to decrease exponentially as well. However, the conduction channel does not shut off abruptly with decreasing gate voltage, but rather decreases at a fixed rate of about 10mV per decade of drain current decrease. For example, for the ALD2108xx device, if the gate threshold voltage is $+0.20V$, the drain current is $10\mu A$ at $V_{GS} = +0.20V$. At $V_{GS} = +0.096V$, the drain current would decrease to $1\mu A$. Extrapolating from this, the drain current is about $0.1\mu A$ at $V_{GS} = 0.00V$, $1nA$ at $V_{GS} = -0.216V$, and so forth. This subthreshold characteristic extends all the way down to current levels below $1nA$ and is limited by junction leakage currents.

At a drain current of “zero current” as defined and selected by the user, the $V_{GS}$ voltage at that zero current can now be estimated. Note that using the above example, with $V_{GS(th)} = +0.20V$, the drain current still hovers around 100nA when the gate is at ground voltage. With a device that has $V_{GS(th)} = +0.40V$ (part number ALD21804), the drain current is about $2nA$ when the gate is at ground potential. Thus, in this case an input signal referenced to ground can operate with a natural drain current of only $2nA$ internal bias current, dissipating nano-watts of power.

LOW POWER AND NANOPower

When supply voltages decrease, the power consumption of a given load resistor decreases as the square of the supply voltage. Thus, one of the benefits in reducing supply voltage is to reduce power consumption. While decreasing power supply voltages and power consumption go hand-in-hand with decreasing useful AC bandwidth and increased noise effects in the circuit, a circuit designer can make the necessary tradeoffs and adjustments in any given circuit design and bias the circuit accordingly for optimal performance.

With EPAD MOSFETs, a circuit that performs any specific function can be designed so that power consumption of that circuit is minimized. These circuits operate in low power mode where the power consumed is measured in mW, uW, and nW (nano-watt) region and still provide a useful and controlled circuit function operation.

ZERO TEMPERATURE COEFFICIENT (ZTC) OPERATION

For an EPAD MOSFET in this product family, operating points exist where the various factors that cause the current to increase as a function of temperature balance out those that cause the current to decrease, thereby canceling each other, and resulting in a net temperature coefficient of near zero. An example of this temperature stable operating point is obtained by a ZTC voltage bias condition, which is $0.38V$ above $V_{G(S)}(th)$ when $V_{GS(on)} = +0.1V$, resulting in a temperature stable current level of about $380\mu A$ for the ALD2108xx and $760\mu A$ for the ALD2129xx devices.

PERFORMANCE CHARACTERISTICS OF EPAD® PRECISION MATCHED PAIR MOSFET FAMILY

Performance characteristics of the EPAD MOSFET product family are shown in the following graphs. In general, the gate threshold voltage shift for each member of the product family causes other affected electrical characteristics to shift linearly with $V_{G(S)}(th)$ bias voltage. This linear shift in $V_{GS}$ causes the subthreshold I-V curves to shift linearly as well. Accordingly, the subthreshold operating current can be determined by calculating the gate source voltage drop relative to its gate threshold voltage, $V_{G(S)}(th)$.

NORMALLY-ON FIXED $R_{DS(ON)}$ AT $V_{GS} =$ GROUND

Several members of this MOSFET family produce a fixed resistance when their gate is grounded. For ALD21800, the drain current at $V_{DS} = 0.1V$ is $10\mu A$ at $V_{GS} = 0.00V$. Thus, just by grounding the gate of the ALD21800, a resistor with $R_{DS(ON)} = 10K\Omega$ is produced (For ALD212900 device, if the gate threshold voltage is $+0.20V$, the drain current is $10\mu A$ at $V_{GS} = +0.20V$. When an ALD214804 gate is grounded, the drain current $I_{DS} = 424\mu A$ @ $V_{DS} = 0.1V$, producing $R_{DS(ON)} = 2.3\Omega$. Similarly, ALD214813 and ALD214835 produces 1.71mA and 3.33mA for each MOSFET, respectively, at $V_{GS} = 0.00V$, producing $R_{DS(ON)}$ values of 59$\Omega$ and 30$\Omega$, respectively. For example, when all 4 MOSFETs in an ALD214835 are connected in parallel, an on-resistance of 30$\Omega/4 = 7.50\Omega$ is measured between the Drain and Source terminals when $V_{GS} = V_{DS} = 0.00V$, producing a fixed on-resistance without any gate bias voltages applied to the device.

MATCHING CHARACTERISTICS

One of the key performance benefits of using matched-pair EPAD MOSFETs is to maintain temperature tracking between the different devices in the same package. In general, for EPAD MOSFET matched pair devices, one device of the matched pair has gate leakage currents, junction temperature effects, and drain current temperature coefficient as a function of bias voltage that cancel out similar effects of the other device, resulting in a temperature stable circuit. As mentioned earlier, this temperature stability can be further enhanced by biasing the matched-pairs at Zero Tempco (ZTC) point, even though that may require special circuit configurations and power consumption design considerations.

POWER SUPPLY SEQUENCES AND ESD CONTROL

EPAD MOSFETs are robust and reliable, as demonstrated by more than a decade of production history supplied to a large installed base of customers across the world. However, these devices do require a few design and handling precautions in order for them to be used successfully.

EPAD MOSFETs, being a CMOS Integrated Circuit, in addition to having Drain, Gate and Source pins normally found in a MOSFET device, have three other types of pins, namely $V+$, $V-$ and IC pins. $V+$ is connected to the substrate, which must always be connected to the most positive supply in a circuit. $V-$ is the body of the MOSFET, which must be connected to the most negative supply voltage in the circuit. IC pins are internally connected pins, which must also be connected to $V-$ Drain, Gate and Source pins must have voltages between $V-$ and $V+$ at all times.

Proper power-up sequencing requires powering up supply voltages before applying any signals. During the power down cycle, remove all signals before removing $V-$ and $V+$. This way internally back biased diodes are never allowed to become forward biased, possibly causing damage to the device. Of course, standard ESD control procedures should also be observed so that static charge does not degrade the performance of the devices.
TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT CHARACTERISTICS

DRAIN SOURCE ON VOLTAGE - VDS(ON) (V)
0 2 4 6 8 10
DRAIN SOURCE ON CURRENT
IDS(ON) (mA)
0 20 60 80 100
VGS = VGS(th) + 0.5V
VGS = VGS(th) + 1.0V
VGS = VGS(th) + 1.5V
VGS = VGS(th) + 2.0V
VGS = VGS(th) + 2.5V
VGS = VGS(th) + 3.0V

LOW VOLTAGE OUTPUT CHARACTERISTICS

DRAIN SOURCE ON VOLTAGE - VDS(ON) (V)
-0.3 -0.2 -0.1 0.0 +0.1 +0.2 +0.3
DRAIN SOURCE ON CURRENT
IDS(ON) (mA)
-10 -20 -30 0 10 20 30
VGS - VGS(th) = 0.5V
V- = 0V
TA = +25°C
VDS = 5V
VGS(th) = +0.4V
VGS(th) = -3.5V
VGS(th) = +1.4V
VGS(th) = -0.4V
VGS(th) = 0.0V
VGS(th) = +0.2V
VGS(th) = -0.8V
VGS(th) = -0.2V
VGS(th) = +0.8V
VGS(th) = -1.3V

FORWARD TRANSFER CHARACTERISTICS

GATE SOURCE VOLTAGE - VGS (V)
-4 0 4 8
DRAIN SOURCE ON CURRENT
IDS(ON) (mA)
100 80 60 40 20 0
TA = +25°C
VDS = 5V

EXPANDED (SUBTHRESHOLD)

GATE SOURCE OVERDRIVE VOLTAGE
VGS - VGS(th) (V)
-5 -4 -3 -2 -1 0 +1 +2
DRAIN SOURCE ON CURRENT
IDS(ON) (nA)
1000000.00 100000.00 10000.00 1000.00 100.00 10.00 1.00 0.10 0.01
TA = +25°C
VDS = 0.1V

FURTHER EXPANDED (SUBTHRESHOLD)

GATE SOURCE OVERDRIVE VOLTAGE
VGS - VGS(th) (V)
-0.5 -0.4 -0.3 -0.2 -0.1 0.0 +0.1 +0.2
DRAIN SOURCE ON CURRENT
IDS(ON) (nA)
1000000.00 100000.00 10000.00 1000.00 100.00 10.00 1.00 0.10 0.01
TA = +25°C
TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

LOW LEVEL OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE

LOW LEVEL OUTPUT CONDUCTANCE vs. GATE THRESHOLD VOLTAGE

HIGH LEVEL OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE

HIGH LEVEL OUTPUT CONDUCTANCE vs. GATE THRESHOLD VOLTAGE

TRANSCONDUCTANCE vs. AMBIENT TEMPERATURE

TRANSCONDUCTANCE vs. GATE THRESHOLD VOLTAGE

\[ V_{GS} = V_{GS(th)} + 0.5V \]

\[ V_{DS} = +3.0V \]

\[ V_{GS} = V_{GS(th)} + 3.0V \]

\[ V_{DS} = +3.0V \]
TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

DRAIN OFF LEAKAGE CURRENT $I_{DS(OFF)}$ vs. AMBIENT TEMPERATURE

OFFSET VOLTAGE vs. AMBIENT TEMPERATURE

REPRESENTATIVE UNITS:

$V_{OS} = V_{GS(th)M1} - V_{GS(th)M2}$
TYPICAL APPLICATIONS

CURRENT SOURCE MIRROR

\[ I_{SOURCE} = I_{SET} = \frac{V^+ - V_t}{R_{SET}} \]

where \( V_t = V_{GS} - V_{GS(th)} = V_{DS} \)

**DIFFERENTIAL AMPLIFIER**

**CURRENT SOURCE MULTIPLICATION**

\[ V^+ = +5V \]

M1, M2: N-Channel MOSFET
M3, M4: P-Channel MOSFET

MSET, M1..MN: N x ALD1101, N x ALD1116, N x ALD1109xx, N x ALD2129xx, N x ALD1103, N x ALD1105, N x ALD1106, N x ALD1108xx, or N x ALD2108xx

All M's in the set are from the same part number.

MSET, M1..MN: N-Channel MOSFET

ALD1102, ALD1117, 1/2 ALD1103, 1/2 ALD1105, 1/2 ALD1106, 1/2 ALD1108xx, or 1/2 ALD2108xx

M1, M2: N-Channel MOSFET
M3, M4: P-Channel MOSFET

M1, M2: ALD1101, ALD1116, ALD1109xx, ALD2129xx, 1/2 ALD1103, 1/2 ALD1105, 1/2 ALD1106, 1/2 ALD1108xx, or 1/2 ALD2108xx

M3, M4: ALD1102, ALD1117, 1/2 ALD1103, 1/2 ALD1105, 1/2 ALD1106, or 1/2 ALD3107xx

**CURRENT SOURCE WITH GATE CONTROL**

**DIGITAL LOGIC CONTROL OF CURRENT SOURCE**

M1: N-Channel MOSFET
M3, M4: P-Channel MOSFET

M1: ALD1101, ALD1116, ALD1109xx, ALD2129xx, 1/2 ALD1103, 1/2 ALD1105, 1/2 ALD1106, 1/2 ALD1108xx, or 1/2 ALD2108xx

M3, M4: ALD1102, ALD1117, 1/2 ALD1103, 1/2 ALD1105, 1/2 ALD1106, or 1/2 ALD3107xx

M1, M2: ALD1101, ALD1116, ALD1109xx, ALD2129xx, 1/2 ALD1103, 1/2 ALD1105, 1/2 ALD1106, 1/2 ALD1108xx, or 1/2 ALD2108xx

Digital Logic Control of Current Source

ON

OFF
TYPICAL APPLICATIONS (cont.)

BASIC CURRENT SOURCES

N-CHANNEL CURRENT SOURCE

\[ I_{\text{SOURCE}} = I_{\text{SET}} = \frac{V^+ - V_t}{R_{\text{SET}}} \]

where \( V_t = V_{GS} - V_{GS(th)} = V_{DS} \)

M1, M2 : N-Channel MOSFET

P-CHANNEL CURRENT SOURCE

\[ I_{\text{SOURCE}} = I_{\text{SET}} = \frac{V^* - 2V_t}{R_{\text{SET}}} \]

where \( V_t = V_{GS} - V_{GS(th)} = V_{DS} \)

M3, M4 : P-Channel MOSFET

CASCODE CURRENT SOURCES

M1, M2, M3, M4 : N-Channel MOSFET

where M1 and M2 is a matched pair and M3 and M4 is a second matched pair.

M1, M2, M3, M4 : P-Channel MOSFET

where M1 and M2 is a matched pair and M3 and M4 is a second matched pair.
SOIC-8 PACKAGE DRAWING

8 Pin Plastic SOIC Package

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.35 - 1.75</td>
<td>0.053 - 0.069</td>
</tr>
<tr>
<td>A₁</td>
<td>0.10 - 0.25</td>
<td>0.004 - 0.010</td>
</tr>
<tr>
<td>b</td>
<td>0.35 - 0.45</td>
<td>0.014 - 0.018</td>
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<tr>
<td>C</td>
<td>0.18 - 0.25</td>
<td>0.007 - 0.010</td>
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<tr>
<td>D-8</td>
<td>4.69 - 5.00</td>
<td>0.185 - 0.196</td>
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<tr>
<td>E</td>
<td>3.50 - 4.05</td>
<td>0.140 - 0.160</td>
</tr>
<tr>
<td>e</td>
<td>1.27 BSC</td>
<td>0.050 BSC</td>
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<tr>
<td>H</td>
<td>5.70 - 6.30</td>
<td>0.224 - 0.248</td>
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<tr>
<td>L</td>
<td>0.60 - 0.937</td>
<td>0.024 - 0.037</td>
</tr>
<tr>
<td>⌀</td>
<td>0° - 8°</td>
<td>0° - 8°</td>
</tr>
<tr>
<td>S</td>
<td>0.25 - 0.50</td>
<td>0.010 - 0.020</td>
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8 Pin Plastic DIP Package

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<th>Millimeters</th>
<th>Inches</th>
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</thead>
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<td>0.105 - 0.200</td>
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<tr>
<td>A₁</td>
<td>0.38 - 1.27</td>
<td>0.015 - 0.050</td>
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<tr>
<td>A₂</td>
<td>1.27 - 2.03</td>
<td>0.050 - 0.080</td>
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<tr>
<td>b</td>
<td>0.89 - 1.65</td>
<td>0.035 - 0.065</td>
</tr>
<tr>
<td>b₁</td>
<td>0.38 - 0.51</td>
<td>0.015 - 0.020</td>
</tr>
<tr>
<td>c</td>
<td>0.20 - 0.30</td>
<td>0.008 - 0.012</td>
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<tr>
<td>D-8</td>
<td>9.40 - 11.68</td>
<td>0.370 - 0.460</td>
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<tr>
<td>E</td>
<td>5.59 - 7.11</td>
<td>0.220 - 0.280</td>
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<tr>
<td>E₁</td>
<td>7.62 - 8.26</td>
<td>0.300 - 0.325</td>
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<tr>
<td>e</td>
<td>2.29 - 2.79</td>
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<tr>
<td>e₁</td>
<td>7.37 - 7.87</td>
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<td>L</td>
<td>2.79 - 3.81</td>
<td>0.110 - 0.150</td>
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<tr>
<td>S-8</td>
<td>1.02 - 2.03</td>
<td>0.040 - 0.080</td>
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<tr>
<td>ø</td>
<td>0° - 15°</td>
<td>0° - 15°</td>
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</tbody>
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