DUAL EPAD® PRECISION HIGH SLEW RATE CMOS OPERATIONAL AMPLIFIER

KEY FEATURES
- Factory pre-trimmed $V_{OS}$
- $V_{OS}=25\mu V$ @ $I_{OS}=0.01pA$
- $5V/\mu s$ slew rate
- EPAD (Electrically Programmable Analog Device)
- User programmable $V_{OS}$ trimmer
- Rail-to-rail input/output
- Compatible with standard EPAD Programmer
- Each amplifier $V_{OS}$ can be trimmed to a different $V_{OS}$ level
- High precision through in-system circuit precision trimming
- Reduces or eliminates $V_{OS}$, PSRR, CMRR and TCVOS errors
- System level “calibration” capability
- Low voltage operation

GENERAL DESCRIPTION
The ALD2724E/ALD2724 is a dual monolithic operational amplifier with MOSFET input that has rail-to-rail input and output voltage ranges. The input voltage range and output voltage range are very close to the positive and negative power supply voltages. Typically the input voltage can be beyond positive power supply voltage $V+$ or the negative power supply voltage $V-$ by up to 300mV. The output voltage swings to within 60mV of either positive or negative power supply voltages at rated load.

With high impedance load, the output voltage of the ALD2724E/ALD2724 approaches within 1mV of the power supply rails. This device is designed as an alternative to the popular J-FET input operational amplifier in applications where lower operating voltages, such as 9V battery or $\pm 3.25V$ to $\pm 5V$ power supplies are being used. The ALD2724E/ALD2724 offers high slew rate of 5.0V/\mu s.

The rail-to-rail input and output feature of the ALD2724E/ALD2724 expands signal voltage range for a given operating supply voltage and allows numerous analog serial stages to be implemented without losing operating voltage margin. The output stage is designed to drive up to 10mA into 400pF capacitive and 1.5K$\Omega$ resistive loads at unity gain and up to 4000pF at a gain of 5. Short circuit protection to either ground or the power supply rails is at approximately 15mA clamp current. Due to complementary output stage design, the output can source and sink 10mA into a load with symmetrical drive and is ideally suited for applications where push-pull voltage drive is desired.

APPLICATIONS
- Sensor interface circuits
- Transducer biasing circuits
- Capacitive and charge integration circuits
- Biochemical probe interface
- Signal conditioning
- Portable instruments
- High source impedance electrode amplifiers
- Precision Sample and Hold amplifiers
- Precision current to voltage converter
- Error correction circuits
- Sensor compensation circuits
- Precision gain amplifiers
- Periodic In-system calibration
- System output level shifter

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Operating Temperature Range</th>
<th>0°C to +70°C</th>
<th>0°C to +70°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-55°C to +125°C</td>
<td>-55°C to +125°C</td>
</tr>
<tr>
<td>14-Pin Small Outline Package (SOIC)</td>
<td>14-Pin Plastic Dip</td>
<td>14-Pin CERDIP</td>
</tr>
<tr>
<td>ALD2724ESB</td>
<td>ALD2724EPB</td>
<td>ALD2724EDB</td>
</tr>
<tr>
<td>ALD2724SB</td>
<td>ALD2724PB</td>
<td>ALD2724DB</td>
</tr>
</tbody>
</table>

* Contact factory for high temperature versions.

BENEFITS
- Ready-to-use off-the-shelf standard part
- Custom automated trimming optional
- Remote controlled automated trimming
- In-System Programming capability
- No external components
- No internal clocking noise source
- Simple and cost effective
- Small package size
- Extremely small total functional volume size
- Low system implementation cost

APPLICATIONS

PIN CONFIGURATION

* N/C Pins are internally connected. Do not connect externally.

Rev 2.1 ©2011 Advanced Linear Devices, Inc. 415 Tasman Drive, Sunnyvale, CA 94089-1706 Tel: (408) 747-1155 Fax: (408) 747-1286 www.aldinc.com
FUNCTIONAL DESCRIPTION

The ALD2724E/ALD2724 uses EPADs as in-circuit elements for trimming of offset voltage bias characteristics. Each ALD2724E/ALD2724 has a pair of EPAD-based circuits connected such that one circuit is used to adjust VOS in one direction and the other circuit is used to adjust VOST in the other direction. While each of the EPAD devices is a monotonically adjustable programmable device, the VOS of the ALD2724E can be adjusted many times in both directions. Once programmed, the set VOS levels are stored permanently, even when the device power is removed.

Functional Description of ALD2724E

The ALD2724E is pre-programmed at the factory under standard operating conditions for minimum equivalent input offset voltage. It also has a guaranteed offset voltage program range, which is ideal for applications that require electrical offset voltage programming.

The ALD2724E is an operational amplifier that can be trimmed with user application-specific programming or in-system programming conditions. User application-specific circuit programming refers to the situation where the Total Input Offset Voltage of the ALD2724E can be trimmed with the actual intended operating conditions.

For example, an application circuit may have +5V and -5V power supplies, and the operational amplifier input is biased at +1V, and an average operating temperature at +85°C. The circuit can be wired up to these conditions within an environmental chamber with the ALD2724E inserted into a test socket connected to this circuit while it is being electrically trimmed. Any error in VOS due to these bias conditions can be automatically zeroed out. The Total VOS error is now limited only by the adjustable range and the stability of VOS, and the input noise voltage of the operational amplifier. Therefore, this Total VOS error now includes VOS as VOS is traditionally specified; plus the VOS error contributions from PSRR, CMRR, TCVOS, and noise. Typically this total VOS error (VOST) is approximately ±25µV for the ALD2724E.

In-System Programming refers to the condition where the EPAD adjustment is made after the ALD2724E has been inserted into a circuit board. In this case, the circuit design must provide for the ALD2724E to operate in normal mode and in programming mode. One of the benefits of in-system programming is that not only is the ALD2724E offset voltage from operating bias conditions accounted for, any residual errors introduced by other circuit components, such as resistor or sensor induced voltage errors, can also be corrected. In this way, the “in-system” circuit output can be adjusted to a desired level, eliminating the need for another trimming function.

Functional Description of ALD2724

The ALD2724 is pre-programmed at the factory under standard operating conditions for minimum equivalent input offset voltage. The ALD2724 offers similar programmable features as the ALD2724E, but with a more limited offset voltage program range. It is intended for standard operational amplifier applications, where little or no electrical programming by the user is necessary.

USER PROGRAMMABLE VOS FEATURE

Each ALD2724E/ALD2724 has four additional pins, compared to a conventional dual operational amplifier which has eight pins. These four additional pins are named VE1A, VE2A for op amp A and VE1B, VE2B for op amp B. Each of these pins VE1A, VE2A, VE1B, VE2B (represented by VExx) are connected to a separate, internal offset bias circuit. VExx pins have initial internal bias voltage values of approximately 1V to 2V. The voltage on these pins can be programmed using the ALD E100 EPAD Programmer and the appropriate Adapter Module. The useful programming range of voltages on VExx pins are 1V to 4V.

VExx pins are programming pins, used during electrical programming mode to inject charge into the internal EPADs. Increasing voltage on VE1A/VE1B decreases the offset voltage whereas increasing voltage on VE2A/VE2B increases the offset voltage of op amp A and op amp B, respectively. The injected charge is then permanently stored. After programming, VExx pins must be left open in order for these voltages to remain at the programmed levels.

During programming, voltages on VExx pins are increased incrementally to program the offset voltage of the operational amplifier to the desired VOS. Note that desired VOS can be any value within the offset voltage programmable ranges, and can be equal zero, a positive value or a negative value. This VOS value can also be reprogrammed to a different value at a later time, provided that the useful VE1x or VE2x programming voltage range has not been exceeded. VExx pins can also serve as capacitively coupled input pins.

Internally, VE1 and VE2 are programmed and connected differentially. Temperature drift effects between the two internal offset bias circuits cancel each other and introduce less net temperature drift coefficient change than offset voltage trimming techniques such as offset adjustment with an external trimmer potentiometer.

While programming, V+, VE1 and VE2 pins may be alternately pulsed with 12V (approximately) pulses generated by the EPAD Programmer. In-system programming requires the ALD2724E application circuit to accommodate these programming pulses. This can be accomplished by adding resistors at certain appropriate circuit nodes. For more information, see Application Note AN1700.
ABSOLUTE MAXIMUM RATINGS
Supply voltage, V+ .................................................. 10.6V
Differential input voltage range ...................................... -0.3V to V+ +0.3V
Power dissipation .................................................... 600 mW
Operating temperature range SB, PB packages .................. 0°C to +70°C
DB package .......................................................... -55°C to +125°C
Storage temperature range ........................................ -65°C to +150°C
Lead temperature, 10 seconds ..................................... +260°C
CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS
\( T_A = 25°C \) \( V_S = \pm 5.0V \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
</table>
| Supply Voltage | V_S | \( \pm 3.25 \) | 6.5 | \( \pm 5.0 \) | 10.0 | \( \pm 3.25 \) | 6.5 | \( \pm 5.0 \) | V | Dual Supply
| Initial Input Offset Voltage | VOS | 25 | 100 | 40 | 150 | \( \mu V \) | RS \( \leq 100K\Omega \) |
| Offset Voltage Program Range | \( \Delta V_{OS} \) | \( \pm 5 \) | \( \pm 7 \) | \( \pm 0.5 \) | \( \pm 2 \) | mV |
| Programmed Input Offset Voltage Error | VOS | 25 | 100 | 40 | 150 | \( \mu V \) | At user specified target offset voltage |
| Total Input Offset Voltage | VOST | 25 | 100 | 40 | 150 | \( \mu V \) | At user specified target offset voltage |
| Input Offset Current | IOS | 0.01 | 10 | 0.01 | 240 | pA | TA = 25°C
| Input Bias Current | IB | 0.01 | 10 | 0.01 | 240 | pA | TA = 25°C
| Input Voltage Range | VR | -0.3 | -2.8 | 5.3 | +2.8 | -0.3 | -2.8 | 5.3 | +2.8 | V | V+ = +5V
| Input Resistance | RIN | \( 10^{14} \) | \( 10^{14} \) | \( \Omega \) | |
| Input Offset Voltage Drift | TCVOS | 5 | 5 | \( \mu V/°C \) | RS \( \leq 100K\Omega \) |
| Initial Power Supply Rejection Ratio | PSRR | 85 | 85 | dB | RS \( \leq 100K\Omega \) |
| Initial Common Mode Rejection Ratio | CMRR | 90 | 90 | dB | RS \( \leq 100K\Omega \) |
| Large Signal Voltage Gain | AV | 150 | 150 | V/mV | RL = 10K\Omega
| | V_O high | 4.998 | 4.99 | V | RL = 1M\Omega V = 5V
| | | | | | | | | | |
| | V_O low | 4.96 | -4.90 | -4.96 | 4.90 | -4.90 | -4.90 | V | RL = 100K\Omega
| | V_O high | 4.95 | 4.95 | V | RL = 100K\Omega
| Output Short Circuit Current | ISC | 15 | 15 | mA |

* NOTES 1 through 9, see section titled “Definitions and Design Notes”. 
OPERATING ELECTRICAL CHARACTERISTICS (cont’d)

\( T_A = 25^\circ C \quad V_S = \pm 5.0V \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>2724E</th>
<th>2724</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Supply Current</strong></td>
<td>I(_S)</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td><strong>Power Dissipation</strong></td>
<td>P(_D)</td>
<td></td>
<td></td>
<td></td>
<td>65</td>
</tr>
<tr>
<td><strong>Input Capacitance</strong></td>
<td>C(_{IN})</td>
<td>1</td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td><strong>Maximum Load Capacitance</strong></td>
<td>C(_L)</td>
<td>400</td>
<td>4000</td>
<td>4000</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Equivalent Input Noise Voltage</strong></td>
<td>e(_n)</td>
<td>26</td>
<td></td>
<td></td>
<td>26</td>
</tr>
<tr>
<td><strong>Equivalent Input Noise Current</strong></td>
<td>i(_n)</td>
<td>0.6</td>
<td></td>
<td></td>
<td>0.6</td>
</tr>
<tr>
<td><strong>Bandwidth</strong></td>
<td>B(_W)</td>
<td>2.1</td>
<td></td>
<td></td>
<td>2.1</td>
</tr>
<tr>
<td><strong>Slew Rate</strong></td>
<td>S(_R)</td>
<td>5.0</td>
<td></td>
<td></td>
<td>5.0</td>
</tr>
<tr>
<td><strong>Rise time</strong></td>
<td>t(_r)</td>
<td>0.1</td>
<td></td>
<td></td>
<td>0.1</td>
</tr>
<tr>
<td><strong>Overshoot Factor</strong></td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td>15</td>
</tr>
<tr>
<td><strong>Settling Time</strong></td>
<td>t(_S)</td>
<td>2</td>
<td></td>
<td></td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Channel Separation</strong></td>
<td>CS</td>
<td>140</td>
<td></td>
<td></td>
<td>140</td>
</tr>
</tbody>
</table>

\( T_A = 25^\circ C \quad V_S = \pm 5.0V \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>2724E</th>
<th>2724</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Average Long Term Input Offset</strong></td>
<td>( \Delta V_{OS}/\Delta \text{time} )</td>
<td>0.02</td>
<td></td>
<td>0.02</td>
<td>( \mu V/1000 \text{hrs} )</td>
</tr>
<tr>
<td><strong>Initial VE Voltage</strong></td>
<td>VE(<em>{1,i}), VE(</em>{2,i})</td>
<td>1.4</td>
<td></td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td><strong>Programmable Change of VE Range</strong></td>
<td>( \Delta V_{E1}, \Delta V_{E2} )</td>
<td>1.5</td>
<td>2.0</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td><strong>Programmed VE Voltage Error</strong></td>
<td>e(VE(<em>{1}-VE</em>{2}))</td>
<td>0.1</td>
<td></td>
<td>0.1</td>
<td>%</td>
</tr>
<tr>
<td><strong>VE Pin Leakage Current</strong></td>
<td>i(_{eb})</td>
<td>-5</td>
<td></td>
<td>-5</td>
<td>( \mu A )</td>
</tr>
</tbody>
</table>

* NOTES 1 through 9, see section titled “Definitions and Design Notes”. 
### OPERATING ELECTRICAL CHARACTERISTICS (cont’d)

**$V_S = \pm 5.0V \ -55°C \leq T_A \leq +125°C$ unless otherwise specified**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>2724E</th>
<th>2724</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial Input offset Voltage</td>
<td>$V_{OS_i}$</td>
<td>0.7</td>
<td>0.7</td>
<td>mV</td>
<td>$R_S \leq 100K\Omega$</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>$I_{OS}$</td>
<td>2.0</td>
<td>2.0</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$I_B$</td>
<td>2.0</td>
<td>2.0</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Initial Power Supply Rejection Ratio $^a$</td>
<td>$PSRR_1$</td>
<td>85</td>
<td>85</td>
<td>dB</td>
<td>$R_S \leq 100K\Omega$</td>
</tr>
<tr>
<td>Initial Common Mode Rejection Ratio $^a$</td>
<td>$CMRR_1$</td>
<td>97</td>
<td>97</td>
<td>dB</td>
<td>$R_S \leq 100K\Omega$</td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>$A_V$</td>
<td>10</td>
<td>25</td>
<td>V/mV</td>
<td>$R_L = 10K\Omega$</td>
</tr>
<tr>
<td>Output Voltage Range</td>
<td>$V_O$</td>
<td>low: 4.8</td>
<td>-4.9</td>
<td>-4.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>high: 4.8</td>
<td>4.9</td>
<td>4.9</td>
<td>$R_L = 10K\Omega$</td>
</tr>
</tbody>
</table>
DEFINITIONS AND DESIGN NOTES:

1. Initial Input Offset Voltage is the initial offset voltage of the ALD2724E/ALD2724 operational amplifier when shipped from the factory. The device has been pre-programmed and tested for programmability.

2. Offset Voltage Program Range is the range of adjustment of user specified target offset voltage. This is typically an adjustment in either the positive or the negative direction of the input offset voltage from an initial input offset voltage. The input offset programming pins, VE1A/VE1B or VE2A/VE2B, change the input offset voltage in the negative or positive direction, for each of the amplifiers, A or B respectively. User specified target offset voltage can be any offset voltage within this programming range.

3. Programmed Input Offset Voltage Error is the final offset voltage error after programming when the Input Offset Voltage is at target Offset Voltage. This parameter is sample tested.

4. Total Input Offset Voltage is the same as Programmed Input Offset Voltage, corrected for system offset voltage error. Usually this is an all inclusive system offset voltage, which also includes offset voltage contributions from input offset voltage, PSRR, CMRR, TCVOS and noise. It can also include errors introduced by external components, at a system level. Programmed Input Offset Voltage and Total Input Offset Voltage is not necessarily zero offset voltage, but an offset voltage set to compensate for other system errors as well. This parameter is sample tested.

5. The Input Offset and Bias Currents are essentially input protection diode reverse bias leakage currents. This low input bias current assures that the analog signal from the source will not be distorted by it. For applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

6. Input Voltage Range is determined by two parallel complementary input stages that are summed internally, each stage having a separate input offset voltage. While Total Input Offset Voltage can be trimmed to a desired target value, it is essential to note that this trimming occurs at only one user selected input bias voltage. Depending on the selected input bias voltage relative to the power supply voltages, offset voltage trimming may affect one or both input stages. For the ALD2724E/ALD2724, the switching point between the two stages occurs at approximately 1.5V above negative supply voltage.

7. Input Offset Voltage Drift is the average change in Total Input Offset Voltage as a function of ambient temperature. This parameter is sample tested.

8. Initial PSRR and initial CMRR specifications are provided as reference information. After programming, error contribution to the offset voltage from PSRR and CMRR is set to zero under the specific power supply and common mode conditions, and becomes part of the Programmed Input Offset Voltage Error.

9. Average Long Term Input Offset Voltage Stability is based on input offset voltage shift through operating life test at 125°C extrapolated to TA = 25°C, assuming activation energy of 1.0eV. This parameter is sample tested.

ADDITIONAL DESIGN NOTES:

A. The ALD2724E/ALD2724 is internally compensated for unity gain stability using a novel scheme which produces a single pole role off in the gain characteristics while providing more than 70 degrees of phase margin at unity gain frequency. A unity gain buffer using the ALD2724E/ALD2724 will typically drive 400pF of external load capacitance.

B. The ALD2724E/ALD2724 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail-to-rail input common mode voltage range. The switching point between the two differential stages is 1.5V above negative supply voltage. For applications such as inverting amplifiers or non-inverting amplifiers with a gain larger than 2.5 (5V operation), the common mode voltage does not make excursions below this switching point. However, this switching does take place if the operational amplifier is connected as a rail-to-rail unity gain buffer and the design must allow for input offset voltage variations.

C. The output stage consists of class AB complementary output drivers. The oscillation resistant feature, combined with the rail-to-rail input and output feature, makes the ALD2724E/ALD2724 an effective analog signal buffer for high source impedance sensors, transducers, and other circuit networks.

D. The ALD2724E/ALD2724 has static discharge protection. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. The user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages not to exceed 0.3V of the power supply voltage levels.

E. VExx are high impedance terminals, as the internal bias currents are set very low to a few microamperes to conserve power. For some applications, these terminals may need to be shielded from external coupling sources. For example, digital signals running nearby may cause unwanted offset voltage fluctuations. Care during the printed circuit board layout, to place ground traces around these pins and to isolate them from digital lines, will generally eliminate such coupling effects. In addition, optional decoupling capacitors of 1000pF or greater value can be added to VExx terminals.

F. The ALD2724E/ALD2724 is designed for use in low voltage, micropower circuits. The maximum operating voltage during normal operation should remain below 10V at all times. Care should be taken to insure that the application in which the device is used does not experience any positive or negative transient voltages that will cause any of the terminal voltages to exceed this limit.

G. All inputs or unused pins except VExx pins should be connected to a supply voltage such as Ground so that they do not become floating pins, since input impedance at these pins is very high. If any of these pins are left undefined, they may cause unwanted oscillation or intermittent excessive current drain. As these devices are built with CMOS technology, normal operating and storage temperature limits, ESD and latchup handling precautions pertaining to CMOS device handling should be observed.
TYPICAL PERFORMANCE CHARACTERISTICS

**COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE**

- Supply Voltage (V) vs. Common Mode Input Voltage Range (V)
  - Supply Voltage Range: ±2 to ±7
  - Temperature: $T_A = 25^\circ C$

**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE**

- Supply Voltage (V) vs. Open Loop Voltage Gain (V/mV)
  - Supply Voltage: ±10 to ±8
  - Temperature: $T_A = -55^\circ C$, $+25^\circ C$, $+125^\circ C$
  - Load Resistors: $R_L = 10K\Omega$, $R_L = 5K\Omega$

**INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE**

- Ambient Temperature (°C) vs. Input Bias Current (μA)
  - Voltage: $V_S = \pm5.0V$
  - Temperature Range: -50 to 125°C

**SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE**

- Supply Voltage (V) vs. Supply Current (mA)
  - Inputs Grounded, Output Unloaded
  - Temperature: $T_A = -55^\circ C$, $-25^\circ C$, $+25^\circ C$, $+80^\circ C$, $+125^\circ C$

**ADJUSTMENT IN INPUT OFFSET VOLTAGE AS A FUNCTION OF CHANGE IN VE1 AND VE2**

- Change in Input Offset Voltage (ΔVos (mV)) vs. Change in VE1 and VE2 (V)
  - ΔVos: -10 to 10
  - Vos: -8 to 8

**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY**

- Frequency (Hz) vs. Open Loop Voltage Gain (dB)
  - Voltage: $V_S = \pm5.0V$
  - Temperature: $T_A = 25^\circ C$
  - Frequency Range: 1 Hz to 100 MHz

**COMMON MODE INPUT VOLTAGE RANGE**

- Supply Voltage (V) vs. Common Mode Input Voltage Range (V)
  - Supply Voltage Range: ±2 to ±7
  - Temperature: $T_A = 25^\circ C$

**INPUT BIAS CURRENT**

- Ambient Temperature (°C) vs. Input Bias Current (μA)
  - Voltage: $V_S = \pm5.0V$
  - Temperature Range: -50 to 125°C

**SUPPLY CURRENT**

- Supply Voltage (V) vs. Supply Current (mA)
  - Inputs Grounded, Output Unloaded
  - Temperature: $T_A = -55^\circ C$, $-25^\circ C$, $+25^\circ C$, $+80^\circ C$, $+125^\circ C$

**ADJUSTMENT IN INPUT OFFSET VOLTAGE**

- Change in Input Offset Voltage (ΔVos (mV)) vs. Change in VE1 and VE2 (V)
  - ΔVos: -10 to 10
  - Vos: -8 to 8

**OPEN LOOP VOLTAGE GAIN**

- Frequency (Hz) vs. Open Loop Voltage Gain (dB)
  - Voltage: $V_S = \pm5.0V$
  - Temperature: $T_A = 25^\circ C$
  - Frequency Range: 1 Hz to 100 MHz

**PHASE SHIFT IN DEGREES**

- Frequency (Hz) vs. Phase Shift (Degrees)
  - Temperature: $T_A = 25^\circ C$
  - Frequency Range: 1 Hz to 100 MHz
TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

LARGE - SIGNAL TRANSIENT RESPONSE

TOTAL INPUT OFFSET VOLTAGE (µV)

-2500 -2000 -1500 -1000 -500 0 500 1000 1500 2000 2500

DISTRIBUTION OF TOTAL INPUT OFFSET VOLTAGE BEFORE AND AFTER EPAD PROGRAMMING

EXAMPLE B:
VOST AFTER EPAD PROGRAMMING
VOST TARGET = -750 µV

EXAMPLE A:
VOST AFTER EPAD PROGRAMMING
VOST TARGET = 0.0 µV

VOST BEFORE EPAD PROGRAMMING

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE

SMALL - SIGNAL TRANSIENT RESPONSE

SUPPLY VOLTAGE (V)

OUTPUT VOLTAGE SWING (V)

0 ±1 ±2 ±3 ±4 ±5 ±6 ±7

-55°C ≤ TA ≤ 125°C
R_L = 10KΩ
R_L = 2KΩ

SUPPLY VOLTAGE (V)

OUTPUT VOLTAGE SWING (V)

-3 -2 -1 0 1 2 3 4 5 6 7

R_L = 2KΩ

R_L = 10KΩ

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE

LOAD RESISTANCE (Ω)

1K 10K 100K 1000K

1000 100 10 1

V_S = ±5.0V
T_A = 25°C

V_S = ±5.0V
T_A = 25°C

R_L = 1.0KΩ
C_L = 50pF

R_L = 1.0KΩ
C_L = 50pF

100mV/div
50mV/div
1µs/div

5V/div
2µs/div

5V/div
2µs/div
TYPICAL PERFORMANCE CHARACTERISTICS (cont’d)

TWO EXAMPLES OF EQUIVALENT INPUT OFFSET VOLTAGE DUE TO
CHANGE IN SUPPLY VOLTAGE vs. SUPPLY VOLTAGE

EXAMPLE A:  
VOS EPAD PROGRAMMED  
AT V_supply = +5V

EXAMPLE B:  
VOS EPAD PROGRAMMED  
AT V_supply = +8V

SUPPLY VOLTAGE (V)

0 1 2 3 4 5 6 7 8 9 10

100
200
300
400
500

EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN SUPPLY VOLTAGE (µV)

THREE EXAMPLES OF EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN COMMON MODE VOLTAGE vs. COMMON MODE VOLTAGE

EXAMPLE A:  
VOS EPAD PROGRAMMED  
AT VIN = 0V

EXAMPLE B:  
VOS EPAD PROGRAMMED  
AT VIN = -4.3V

EXAMPLE C:  
VOS EPAD PROGRAMMED  
AT VIN = +5V

COMMON MODE VOLTAGE (V)

-5 -4 -3 -2 -1 0 1 2 3 4 5

100
200
300
400
500

EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN COMMON MODE VOLTAGE (µV)

EXAMPLE OF MINIMIZING EQUIVALENT INPUT OFFSET VOLTAGE FOR A COMMON MODE VOLTAGE RANGE OF 0.5V

COMMON MODE VOLTAGE RANGE OF 0.5V

VOS EPAD PROGRAMMED  
AT COMMON MODE VOLTAGE OF 0.25V

COMMON MODE VOLTAGE (V)

-0.5 -0.4 -0.3 -0.2 -0.1 0.0 0.1 0.2 0.3 0.4 0.5

10
20
30
40
50

EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN COMMON MODE VOLTAGE (µV)
TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

APPLICATION SPECIFIC / IN-SYSTEM PROGRAMMING

Examples of applications where accumulated total input offset voltage from various contributing sources is minimized under different sets of user-specified operating conditions

EXAMPLE A

EXAMPLE B

EXAMPLE C

EXAMPLE D

- Device input $V_{OS}$
- PSRR equivalent $V_{OS}$
- CMRR equivalent $V_{OS}$
- $T_A$ equivalent $V_{OS}$
- Noise equivalent $V_{OS}$
- External Error equivalent $V_{OS}$

TOTAL INPUT VOLTAGE ($\mu$V)

TOTAL INPUT OFFSET VOLTAGE ($\mu$V)

VOS BUDGET BEFORE EPAD PROGRAMMING

VOS BUDGET AFTER EPAD PROGRAMMING

VOS BUDGET BEFORE EPAD PROGRAMMING

VOS BUDGET AFTER EPAD PROGRAMMING

VOS BUDGET BEFORE EPAD PROGRAMMING

VOS BUDGET AFTER EPAD PROGRAMMING

VOS BUDGET BEFORE EPAD PROGRAMMING

VOS BUDGET AFTER EPAD PROGRAMMING
### 14 Pin Plastic SOIC Package

#### Dimensions Table

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.35 - 1.75</td>
<td>0.053 - 0.069</td>
</tr>
<tr>
<td>A_1</td>
<td>0.10 - 0.25</td>
<td>0.004 - 0.010</td>
</tr>
<tr>
<td>b</td>
<td>0.35 - 0.45</td>
<td>0.014 - 0.018</td>
</tr>
<tr>
<td>C</td>
<td>0.18 - 0.25</td>
<td>0.007 - 0.010</td>
</tr>
<tr>
<td>D-14</td>
<td>8.55 - 8.75</td>
<td>0.336 - 0.345</td>
</tr>
<tr>
<td>E</td>
<td>3.50 - 4.05</td>
<td>0.140 - 0.160</td>
</tr>
<tr>
<td>e</td>
<td>1.27 BSC</td>
<td>0.050 BSC</td>
</tr>
<tr>
<td>H</td>
<td>5.70 - 6.30</td>
<td>0.224 - 0.248</td>
</tr>
<tr>
<td>L</td>
<td>0.60 - 0.937</td>
<td>0.024 - 0.037</td>
</tr>
<tr>
<td>ø</td>
<td>0° - 8°</td>
<td>0° - 8°</td>
</tr>
<tr>
<td>S</td>
<td>0.25 - 0.50</td>
<td>0.010 - 0.020</td>
</tr>
</tbody>
</table>
PDIP-14 PACKAGE DRAWING

14 Pin Plastic DIP Package

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A_1</td>
<td>3.81</td>
<td>5.08</td>
</tr>
<tr>
<td>A_2</td>
<td>1.27</td>
<td>2.03</td>
</tr>
<tr>
<td>b</td>
<td>0.89</td>
<td>1.65</td>
</tr>
<tr>
<td>b_1</td>
<td>0.38</td>
<td>0.51</td>
</tr>
<tr>
<td>c</td>
<td>0.20</td>
<td>0.30</td>
</tr>
<tr>
<td>D-14</td>
<td>17.27</td>
<td>19.30</td>
</tr>
<tr>
<td>E</td>
<td>5.59</td>
<td>7.11</td>
</tr>
<tr>
<td>E_1</td>
<td>7.62</td>
<td>8.26</td>
</tr>
<tr>
<td>e</td>
<td>2.29</td>
<td>2.79</td>
</tr>
<tr>
<td>e_1</td>
<td>7.37</td>
<td>7.87</td>
</tr>
<tr>
<td>L</td>
<td>2.79</td>
<td>3.81</td>
</tr>
<tr>
<td>S-14</td>
<td>1.02</td>
<td>2.03</td>
</tr>
<tr>
<td>ø</td>
<td>0°</td>
<td>15°</td>
</tr>
</tbody>
</table>
### CERDIP-14 PACKAGE DRAWING

14 Pin CERDIP Package

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>3.55</td>
<td>5.08</td>
</tr>
<tr>
<td>A₁</td>
<td>1.27</td>
<td>2.16</td>
</tr>
<tr>
<td>b</td>
<td>0.97</td>
<td>1.65</td>
</tr>
<tr>
<td>b₁</td>
<td>0.36</td>
<td>0.58</td>
</tr>
<tr>
<td>C</td>
<td>0.20</td>
<td>0.38</td>
</tr>
<tr>
<td>D-14</td>
<td>--</td>
<td>19.94</td>
</tr>
<tr>
<td>E</td>
<td>5.59</td>
<td>7.87</td>
</tr>
<tr>
<td>E₁</td>
<td>7.73</td>
<td>8.26</td>
</tr>
<tr>
<td>e</td>
<td>2.54 BSC</td>
<td>0.100 BSC</td>
</tr>
<tr>
<td>e₁</td>
<td>7.62 BSC</td>
<td>0.300 BSC</td>
</tr>
<tr>
<td>L</td>
<td>3.81</td>
<td>5.08</td>
</tr>
<tr>
<td>L₁</td>
<td>3.18</td>
<td>--</td>
</tr>
<tr>
<td>L₂</td>
<td>0.38</td>
<td>1.78</td>
</tr>
<tr>
<td>S</td>
<td>--</td>
<td>2.49</td>
</tr>
<tr>
<td>Ø</td>
<td>0°</td>
<td>15°</td>
</tr>
</tbody>
</table>

Millimeters and Inches dimensions are given for the 14 Pin CERDIP Package.