GENERAL DESCRIPTION

ALD310702A/ALD310702 high precision monolithic quad P-Channel MOSFET arrays are matched at the factory using ALD’s proven EPAD® CMOS technology. This device is available in a quad version and is a member of the EPAD® Matched Pair MOSFET Family. The ALD310702A/ALD310702 is a P-channel version of the popular ALD110802A/ALD110802 Precision Threshold device. Together, these two MOSFET series enable complementary precision N-Channel and P-Channel MOSFET array based circuits.

Intended for low voltage and low power small signal applications, the ALD310702A/ALD310702 features precision -0.20V Gate Threshold Voltage, which enables circuit designs with very low operating voltages such as < +0.5V power supplies where the circuits operate below the threshold voltage of the ALD310702A/ALD310702. This feature also enhances input/output signal operating ranges, especially in very low operating voltage environments. With these low threshold precision devices, a circuit with multiple cascading stages can be constructed to operate at extremely low supply or bias voltage levels. ALD310702A/ALD310702 also features high input impedance (2.5 x 10¹⁰ Ω) and high DC current gain (>10⁸).

ALD310702A/ALD310702 MOSFETs are designed for exceptional matching of device electrical characteristics. The Gate Threshold Voltage $V_{GS(th)}$ is set precisely at -0.20V +/-0.02V, featuring a typical offset voltage of only +/-0.001V (1mV). As these devices are on the same monolithic chip, they also exhibit excellent temperature tracking characteristics. They are versatile design components for a broad range of precision analog applications such as basic building blocks for current mirrors, matching circuits, current sources, differential amplifier input stages, transmission gates, and multiplexers. These devices also excel in limited operating voltage applications such as very low level precision voltage-clamps. In addition to matched pair electrical characteristics, each individual MOSFET exhibits individual well controlled manufacturing characteristics, enabling the user to depend on tight design limits from different production batches.

APPLICATIONS

- 0.5% precision current mirrors and current sources
- Low Tempco (<= 50ppm/°C) current mirrors/sources
- Energy harvesting circuits
- Very low voltage analog and digital circuits
- Backup battery circuits & power failure detectors
- Precision low level voltage-clamps
- Low level zero-crossing detector
- Source followers and buffers
- Precision capacitive probes and sensor interfaces
- Precision charge detectors and charge integrators
- Discrete differential amplifier input stage
- Peak-detectors and level-shifters
- High-side switches and Sample-and-Hold switches
- Precision current multipliers
- Discrete analog switches / multiplexers
- Discrete voltage comparators

FEATURES & BENEFITS

- Precision matched Gate Threshold Voltages
- Precision offset voltages (VOS):
  - ALD310702A: 2mV max.
  - ALD310702: 10mV max.
- Sub-threshold voltage operation
- Low min. operating voltage of less than 0.2V
- Ultra low min. operating current of less than 1nA
- Nano-power operation
- Wide dynamic operating current ranges
- Exponential operating current ranges
- Matched transconductance and output conductance
- Matched and tracked temperature characteristics
- Tight lot-to-lot parametric control
- Positive, zero, and negative $V_{GS(th)}$ tempco bias currents
- Low input capacitance
- Low input/output leakage currents

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Package</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-Pin SOIC</td>
<td>16-Pin Plastic Dip Package</td>
</tr>
<tr>
<td>ALD310702ASCL</td>
<td>ALD310702APCL</td>
</tr>
<tr>
<td>ALD310702SCL</td>
<td>ALD310702PCL</td>
</tr>
</tbody>
</table>

*Contact factory for industrial temp. range or user-specified threshold voltage values.

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GENERAL DESCRIPTION (cont.)

These devices are built to offer minimum offset voltage and differential thermal response, and they can also be used for switching and amplifying applications in -0.40V to -8.0V (±0.20V to ±4.0V) powered systems where low input bias current, low input capacitance, and fast switching speed are desired. These devices, exhibiting well controlled turn-off and sub-threshold characteristics, operate the same as standard enhancement mode P-Channel MOSFETs. However, the precision of the Gate Threshold Voltage enable two key additional characteristics, or operating features. First, the operating current level varies exponentially with gate bias voltage at or below the Gate Threshold Voltage (subthreshold region). Second, the circuit can be biased and operated in the subthreshold region with nA of bias current and nW of power dissipation.

For most general applications, connect the V+ pin to the most positive voltage and the V- and IC (internally-connected) pins to the most negative voltage in the system. All other pins must have voltages within these voltage limits at all times. Standard ESD protection facilities and procedures for static sensitive devices are required when handling these devices.

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
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</thead>
<tbody>
<tr>
<td>Drain-Source voltage</td>
<td>V_DS</td>
<td>-8.0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate-Source voltage</td>
<td>V_GS</td>
<td>-8.0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Operating Current</td>
<td></td>
<td></td>
<td>80mA</td>
<td></td>
<td></td>
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<tr>
<td>Power dissipation</td>
<td></td>
<td></td>
<td>500mW</td>
<td></td>
<td></td>
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<tr>
<td>Operating temperature range</td>
<td>SCL, PCL</td>
<td>0°C</td>
<td>+70°C</td>
<td></td>
<td>-65°C</td>
<td>+150°C</td>
<td>+260°C</td>
<td></td>
<td></td>
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</tbody>
</table>

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>ALD310702A</th>
<th>ALD310702</th>
<th>Unit</th>
<th>Test Conditions</th>
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</thead>
<tbody>
<tr>
<td>Gate Threshold Voltage</td>
<td>V_GS(th)</td>
<td>-0.22</td>
<td>-0.20</td>
<td>-0.18</td>
<td>V DS = -1µA, VDS = -0.1V</td>
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<tr>
<td>Offset Voltage</td>
<td>V_OS</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>10 mV</td>
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<tr>
<td>Gate Threshold Temperature</td>
<td>TCVGSM(th)</td>
<td>-2</td>
<td>-2</td>
<td></td>
<td>mV/°C</td>
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<tr>
<td>Drain Source On Current</td>
<td>IDS(ON)</td>
<td>-2.03</td>
<td>-2.03</td>
<td></td>
<td>mA VGS = VDS = -5.0V</td>
</tr>
<tr>
<td>Transconductance Current</td>
<td>G_FS</td>
<td>570</td>
<td>570</td>
<td></td>
<td>µA/V VGS = VDS = -5.0V</td>
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<tr>
<td>Transconductance Mismatch</td>
<td>ΔG_FS</td>
<td>1</td>
<td>1</td>
<td>%</td>
<td>VGS = VDS = -5.0V</td>
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<tr>
<td>Output Conductance</td>
<td>G_O S</td>
<td>48</td>
<td>48</td>
<td>µA/V</td>
<td>VGS(th) = -4.0V, VDS = -5.0V</td>
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<tr>
<td>Drain Source On Resistance</td>
<td>R_D(S(ON))</td>
<td>1.14</td>
<td>1.14</td>
<td>KΩ</td>
<td>VGS = -5.0V, VDS = -0.1V</td>
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<tr>
<td>Drain Source On Resistance Mismatch</td>
<td>ΔR_D(S(ON))</td>
<td>1</td>
<td>1</td>
<td>%</td>
<td></td>
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<tr>
<td>Drain Source Breakdown</td>
<td>B_VDSX</td>
<td>-8.0</td>
<td>-8.0</td>
<td>V</td>
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<tr>
<td>Drain Source Leakage Current</td>
<td>IDS (OFF)</td>
<td>400</td>
<td>400</td>
<td>pA</td>
<td></td>
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<tr>
<td>Gate Leakage Current</td>
<td>I_GSS</td>
<td>200</td>
<td>200</td>
<td>pA</td>
<td></td>
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<tr>
<td>Input Capacitance</td>
<td>C_ISS</td>
<td>2.5</td>
<td>2.5</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

Notes:  
1 Consists of junction leakage currents  
2 Sample tested parameters
**TYPICAL PERFORMANCE CHARACTERISTICS**

**OUTPUT CHARACTERISTICS**

**FORWARD TRANSFER CHARACTERISTICS**

**LOW VOLTAGE OUTPUT CHARACTERISTICS**

**DRAIN SOURCE ON CURRENT vs. GATE AND DRAIN SOURCE VOLTAGE**

- **DRAIN SOURCE ON VOLTAGE - VDS(ON) (V)**
  - Drain Source On Current - IDS(ON) (µA)
  - Drain Source Voltage - VDS(ON) (V)
  - Gate Voltage - VGS (V)

- **DRAIN SOURCE ON CURRENT vs. GATE AND DRAIN SOURCE VOLTAGE**
  - Drain Source Current - IDS(ON) (µA)
  - Gate and Drain Source Voltage - VGS (V)

- **TYPICAL PERFORMANCE CHARACTERISTICS**
  - Drain Source On Voltage - VDS(ON) (V)
  - Drain Source On Current - IDS(ON) (µA)
  - Gate and Drain Source Voltage - VGS (V)

- **FORWARD TRANSFER CHARACTERISTICS (SUBTHRESHOLD)**
  - Drain Source Current - IDS(ON) (µA)
  - Gate Source Voltage - VGS (V)
  - Drain Source Voltage - VDS(ON) (V)

- **OUTPUT CHARACTERISTICS**
  - Drain Source On Current - IDS(ON) (µA)
  - Drain Source Voltage - VDS(ON) (V)
  - Gate Voltage - VGS (V)
TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

FORWARD TRANSFER CHARACTERISTICS
EXPANDED (SUBTHRESHOLD)

GATE THRESHOLD VOLTAGE

VGS(th) (V)

V- = -5V

TA = +25°C

FORWARD TRANSFER CHARACTERISTICS
FURTHER EXPANDED (SUBTHRESHOLD)

GATE THRESHOLD VOLTAGE

VGS(th) (V)

VDS = -5V

TA = +25°C

GATE THRESHOLD VOLTAGE
vs. SUBSTRATE BIAS

VGS(th) (V)

SUBSTRATE BIAS - V+ (V)

GATE THRESHOLD VOLTAGE
vs. V- VOLTAGE

VGS(th) (V)

V- VOLTAGE (V)

GATE THRESHOLD VOLTAGE
vs. AMBIENT TEMPERATURE

VGS(th) (V)

AMBIENT TEMPERATURE - TA (°C)

FORWARD TRANSFER CHARACTERISTICS
FURTHER EXPANDED (SUBTHRESHOLD)

DRAIN SOURCE ON CURRENT
IDS(ON) (µA)

GATE SOURCE OVERDRIVE VOLTAGE
VGS - VGS(th) (V)

VDS = -5V

TA = +25°C

VDS = -0.1V

V+ = 0V

V- = -5V

TA = +25°C

VDS = -5V

TA = +25°C

ALD310702: VGS(th) = -0.200V

ALD310704: VGS(th) = -0.400V

ALD310700: VGS(th) = 0.000V

ALD310702: VGS(th) = -0.800V

ALD310708: VGS(th) = -0.900V

ALD310704: VGS(th) = 0.500V

ALD310700: VGS(th) = 0.000V

ALD310702: VGS(th) = -0.900V

ALD310708: VGS(th) = -0.800V

ALD310700: VGS(th) = -0.400V

ALD310704: VGS(th) = -0.500V

ALD310702: VGS(th) = -0.200V

ALD310708: VGS(th) = -0.700V

ALD310700: VGS(th) = -0.100V

ALD310704: VGS(th) = -0.300V

ALD310702: VGS(th) = -0.100V

ALD310708: VGS(th) = -0.600V

ALD310700: VGS(th) = -0.100V

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ALD310702: VGS(th) = -0.200V

ALD310708: VGS(th) = -0.700V

ALD310700: VGS(th) = -0.100V

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ALD310704: VGS(th) = -0.300V

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ALD310702: VGS(th) = -0.100V

ALD310708: VGS(th) = -0.600V

ALD310700: VGS(th) = -0.100V

ALD310704: VGS(th) = -0.300V

ALD310702: VGS(th) = -0.100V

ALD310708: VGS(th) = -0.600V

ALD310700: VGS(th) = -0.100V
TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

**TRANSCONDUCTANCE vs. AMBIENT TEMPERATURE**

![Graph showing transconductance vs. ambient temperature](image)

** TRANSCONDUCTANCE **

- $GFS \ (\mu A/V)$
- $VDS = -0.1V$
- $V+ = 0V$
- $V- = -5V$

**GATE THRESHOLD VOLTAGE**

- $V+ = 0V$
- $V- = -5V$

**TRANSCONDUCTANCE vs. GATE SOURCE OVERVOLTAGE**

![Graph showing transconductance vs. gate source overvoltage](image)

** TRANSCONDUCTANCE **

- $VGS = VGS(th) - 4.0V$
- $VGS = VGS(th) - 1.0V$
- $VGS = VGS(th) - 0.5V$

**AMBIENT TEMPERATURE**

- $TA \ (°C)$

**OUTPUT CONDUCTANCE vs. DRAIN SOURCE ON VOLTAGE**

![Graph showing output conductance vs. drain source on voltage](image)

** OUTPUT CONDUCTANCE **

- $GDS \ (\mu A/V)$
- $VGS(th) - 4.0V$
- $VGS(th) - 1.0V$
- $VGS(th) - 0.5V$

**ZERO TEMPERATURE COEFFICIENT (ZTC)**

![Graph showing zero temperature coefficient](image)

** DRAIN SOURCE ON CURRENT **

- $ID(ON) \ (\mu A)$
- $VDS = -0.1V$
- $V+ = 0V$
- $V- = -5V$

**GATE SOURCE OVERDRIVE VOLTAGE**

- $VGS - VGS(th) \ (V)$
- $VGS = VGS(th) - 4.0V$
- $VDS = -5.0V$
- $VGS = VGS(th) - 1.0V$
- $VDS = -5.0V$
- $VGS = VGS(th) - 0.5V$
- $VDS = -5.0V$

**OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE**

![Graph showing output conductance vs. ambient temperature](image)

** OUTPUT CONDUCTANCE **

- $GDS \ (\mu A/V)$
- $VGS(th) - 4.0V$
- $VGS(th) - 1.0V$
- $VGS(th) - 0.5V$
TYPICAL APPLICATIONS

LOW VOLTAGE CURRENT SOURCE MIRROR

\[ I_{\text{SOURCE}} = I_{\text{SET}} \frac{V_{\text{SET}}}{R_{\text{SET}}} \]

M1, M2: N-Channel MOSFET
M3, M4: P-Channel MOSFET

LOW VOLTAGE DIFFERENTIAL AMPLIFIER

\[ V_{\text{IN}} = \frac{V_{\text{OUT}}}{1 + R_{\text{IN}}/R_{\text{OUT}}} \]

M1, M2: N-Channel MOSFET
M3, M4: P-Channel MOSFET

0.5% PRECISION LOW VOLTAGE CURRENT SOURCE MULTIPLICATION

\[ I_{\text{SOURCE}} = I_{\text{SET}} \cdot X \]

MNSET: MN1, MN2, MNX: N-Channel MOSFET
MPSET: MP1, MP2, MPY: P-Channel MOSFET
TYPICAL APPLICATIONS (cont.)

0.5% LOW VOLTAGE PRECISION CURRENT MIRRORS

\[ ISOURCE = ISET = \frac{V^+ - V_t}{R_{\text{SET}}} \]

M1, M2: N-Channel MOSFET

M3, M4: P-Channel MOSFET

0.5% PRECISION LOW VOLTAGE CASCODE CURRENT SOURCES

\[ ISOURCE = 3 \cdot ISET = 3 \left( \frac{V^+ - 2V_t}{R_{\text{SET}}} \right) \]

MPA1...MPA4: ALD310702 P-Channel MOSFET (1st individual pkg)
MPB1...MPB4: ALD310702 P-Channel MOSFET (2nd individual pkg)

0.5% PRECISION LOW TEMPCO CASCODE CURRENT SOURCES

\[ ISOURCE = ISET = \frac{V^+ - 2V_t}{R_{\text{SET}}} \]

Temperature stable <= 50ppm/°C when ISET = 57µA.
SOIC-16 PACKAGE DRAWING

16 Pin Plastic SOIC Package

<table>
<thead>
<tr>
<th></th>
<th>Millimeters</th>
<th>Inches</th>
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<tbody>
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### PDIP-16 PACKAGE DRAWING

#### 16 Pin Plastic DIP Package

![Diagram of PDIP-16 Package](image)

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<thead>
<tr>
<th>Dim</th>
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<th>Inches</th>
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<tr>
<td>A</td>
<td>3.81 - 5.08</td>
<td>0.105 - 0.200</td>
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<tr>
<td>A₁</td>
<td>0.38 - 1.27</td>
<td>0.015 - 0.050</td>
</tr>
<tr>
<td>A₂</td>
<td>1.27 - 2.03</td>
<td>0.050 - 0.080</td>
</tr>
<tr>
<td>b</td>
<td>0.89 - 1.65</td>
<td>0.035 - 0.065</td>
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<tr>
<td>b₁</td>
<td>0.38 - 0.51</td>
<td>0.015 - 0.020</td>
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<tr>
<td>c</td>
<td>0.20 - 0.30</td>
<td>0.008 - 0.012</td>
</tr>
<tr>
<td>D-16</td>
<td>18.93 - 21.33</td>
<td>0.745 - 0.840</td>
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<tr>
<td>E</td>
<td>5.59 - 7.11</td>
<td>0.220 - 0.280</td>
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<tr>
<td>E₁</td>
<td>7.62 - 8.26</td>
<td>0.300 - 0.325</td>
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