GENERAL DESCRIPTION
ALD310708A/ALD310708 high precision monolithic quad P-Channel MOSFET arrays are matched at the factory using ALD’s proven EPAD® CMOS technology. This device is available in a quad version and is a member of the EPAD® Matched Pair MOSFET Family. The ALD310708A/ALD310708 is a P-channel version of the popular ALD110808A/ALD110808 Precision Threshold device. Together, these two MOSFET series enable complementary precision N-Channel and P-Channel MOSFET array based circuits.

Intended for low voltage and low power small signal applications, the ALD310708A/ALD310708 features precision -0.80V Gate Threshold Voltage, which enables circuit designs with very low operating voltages such as 2V power supplies where the circuits operate below the threshold voltage of the ALD310708A/ALD310708. This feature also enhances input/output signal operating ranges, especially in very low operating voltage environments. With these low threshold precision devices, a circuit with multiple cascading stages can be constructed to operate at extremely low supply or bias voltage levels. ALD310708A/ALD310708 also features high input impedance (2.5 x 10¹⁰ Ω) and high DC current gain (>10⁸).

ALD310708A/ALD310708 MOSFETs are designed for exceptional matching of device electrical characteristics. The Gate Threshold Voltage VGS(th) is set precisely at -0.80V +/-0.02V, featuring a typical offset voltage of only +/-0.001V (1mV). As these devices are on the same monolithic chip, they also exhibit excellent temperature tracking characteristics. They are versatile design components for a broad range of precision analog applications such as basic building blocks for current mirrors, matching circuits, current sources, differential amplifier input stages, transmission gates, and multiplexers. These devices also excel in limited operating voltage applications such as very low level precision voltage-clamps. In addition to matched pair electrical characteristics, each individual MOSFET exhibits individual well controlled manufacturing characteristics, enabling the user to depend on tight design limits from different production batches.

APPLICATIONS
• 0.5% precision current mirrors and current sources
• Low Tempco (<= 50ppm/°C) current mirrors/sources
• Energy harvesting circuits
• Very low voltage analog and digital circuits
• Backup battery circuits & power failure detectors
• Precision low level voltage-clamps
• Low level zero-crossing detector
• Source followers and buffers
• Precision capacitive probes and sensor interfaces
• Precision charge detectors and charge integrators
• Discrete differential amplifier input stage
• Peak-detectors and level-shifters
• High-side switches and Sample-and-Hold switches
• Precision current multipliers
• Discrete analog switches / multiplexers
• Discrete voltage comparators

FEATURES & BENEFITS
• Precision matched Gate Threshold Voltages
• Precision offset voltages (VOS):
  ALD310708A: 2mV max.
  ALD310708: 10mV max.
• Sub-threshold voltage operation
• Low min. operating voltage of less than 0.8V
• Ultra low min. operating current of less than 1nA
• Nano-power operation
• Wide dynamic operating current ranges
• Exponential operating current ranges
• Matched transconductance and output conductance
• Matched and tracked temperature characteristics
• Tight lot-to-lot parametric control
• Positive, zero, and negative VGS(th) tempco bias currents
• Low input capacitance
• Low input/output leakage currents

ORDERING INFORMATION
(*L* suffix denotes lead-free (RoHS))

<table>
<thead>
<tr>
<th>Operating Temperature Range *</th>
<th>0°C to +70°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-Pin SOIC Package</td>
<td>16-Pin Plastic Dip Package</td>
</tr>
<tr>
<td>ALD310708A SCL</td>
<td>ALD310708APCL</td>
</tr>
<tr>
<td>ALD310708B SCL</td>
<td>ALD310708PCL</td>
</tr>
</tbody>
</table>

*Contact factory for industrial temp. range or user-specified threshold voltage values.

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GENERAL DESCRIPTION (cont.)

These devices are built to offer minimum offset voltage and differential thermal response, and they can also be used for switching and amplifying applications in -0.80V to -8.0V (+/-0.40V to +/-4.0V) powered systems where low input bias current, low input capacitance, and fast switching speed are desired. These devices, exhibiting well controlled turn-off and sub-threshold characteristics, operate the same as standard enhancement mode P-Channel MOSFETs. However, the precision of the Gate Threshold Voltage enable two key additional characteristics, or operating features. First, the operating current level varies exponentially with gate bias voltage at or below the Gate Threshold Voltage (subthreshold region). Second, the circuit can be biased and operated in the subthreshold region with nA of bias current and nW of power dissipation.

For most general applications, connect the V+ pin to the most positive voltage and the V- and IC (internally-connected) pins to the most negative voltage in the system. All other pins must have voltages within these voltage limits at all times. Standard ESD protection facilities and procedures for static sensitive devices are required when handling these devices.

ABSOLUTE MAXIMUM RATINGS

- Drain-Source voltage, \( V_{DS} \) 
- Gate-Source voltage, \( V_{GS} \)
- Operating Current 
- Power dissipation
- Operating temperature range SCL, PCL
- Storage temperature range
- Lead temperature, 10 seconds

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

\( V^+ = +5V \quad V^- = GND \quad T_A = 25^\circ C \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>ALD310708A</th>
<th>ALD310708</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Threshold Voltage</td>
<td>( V_{GS(th)} )</td>
<td>-0.82</td>
<td>-0.80</td>
<td>-0.78</td>
<td>V</td>
</tr>
<tr>
<td>Offset Voltage</td>
<td>( V_{OS} )</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>mV</td>
</tr>
<tr>
<td>Gate Threshold Temperature</td>
<td>( TCV_{GS(th)} )</td>
<td>-2</td>
<td>-2</td>
<td>mV/°C</td>
<td></td>
</tr>
<tr>
<td>Drain Source On Current</td>
<td>( I_{DS(ON)} )</td>
<td>-1.65</td>
<td>-1.65</td>
<td>mA</td>
<td>( V_{GS} = V_{DS} = -5.0V )</td>
</tr>
<tr>
<td>Transconductance Current</td>
<td>( G_F )</td>
<td>570</td>
<td>570</td>
<td>( \mu A/V )</td>
<td>( V_{GS} = V_{DS} = -5.0V )</td>
</tr>
<tr>
<td>Transconductance Mismatch</td>
<td>( \Delta G_F )</td>
<td>1</td>
<td>1</td>
<td>%</td>
<td>( V_{GS} = V_{DS} = -5.0V )</td>
</tr>
<tr>
<td>Output Conductance</td>
<td>( G_O )</td>
<td>48</td>
<td>48</td>
<td>( \mu A/V )</td>
<td>( V_{GS(th)} = -4.0V, V_{DS} = -5.0V )</td>
</tr>
<tr>
<td>Drain Source On Resistance</td>
<td>( R_{DS(ON)} )</td>
<td>1.25</td>
<td>1.25</td>
<td>KΩ</td>
<td>( V_{GS} = -5.0V, V_{DS} = -0.1V )</td>
</tr>
<tr>
<td>Drain Source On Resistance Mismatch</td>
<td>( \Delta R_{DS(ON)} )</td>
<td>1</td>
<td>1</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Drain Source Breakdown</td>
<td>( BVDX )</td>
<td>-8.0</td>
<td>-8.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Drain Source Leakage Current</td>
<td>( I_{DS \ (OFF)} )</td>
<td>400</td>
<td>400</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>Gate Leakage Current</td>
<td>( I_{GS} )</td>
<td>200</td>
<td>200</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>( C_{ISS} )</td>
<td>2.5</td>
<td>2.5</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

Notes: 1. Consists of junction leakage currents
2. Sample tested parameters
TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT CHARACTERISTICS

- Drain source on voltage - \(V_{DS(ON)}\) (V)
- Drain source on current - \(I_{DS(ON)}\) (\(\mu\)A)

LOW VOLTAGE OUTPUT CHARACTERISTICS

- Drain source on voltage - \(V_{DS(ON)}\) (V)
- Drain source on current - \(I_{DS(ON)}\) (\(\mu\)A)

FORWARD TRANSFER CHARACTERISTICS

- Gate source voltage - \(V_{GS}\) (V)
- Drain source on current - \(I_{DS(ON)}\) (\(\mu\)A)

DRAIN SOURCE ON CURRENT vs. GATE AND DRAIN SOURCE VOLTAGE

- Gate and drain source voltage - \(V_{GS}\) (V)
- Drain source on current - \(I_{DS(ON)}\) (\(\mu\)A)
TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

**GATE THRESHOLD VOLTAGE vs. DRAIN SOURCE VOLTAGE**

- **Vgs(th)** (V)
  - 0.800V (ALD310708)
  - 0.400V (ALD310704)
  - 0.000V (ALD310700)
  - -0.200V (ALD310702)

- **Vds** = -0.1V
- **V+** = 0V
- **V-** = -5V
- **TA** = +25°C

**GATE THRESHOLD VOLTAGE vs. AMBIENT TEMPERATURE**

- **Vgs(th)** (V)
  - ALD310708: -0.800V
  - ALD310704: -0.400V
  - ALD310700: 0.000V
  - ALD310702: -0.200V

- **Vds** = -5V
- **V+** = 0V
- **V-** = -5V
- **TA** = +25°C

**FORWARD TRANSFER CHARACTERISTICS EXPANDED (SUBTHRESHOLD)**

- **DRAIN SOURCE VOLTAGE - Vds (V)**
- **GATE SOURCE VOLTAGE - Vgs (V)**

- **IDS(ON)** (µA)
  - 100000
  - 10000
  - 1000
  - 100
  - 10
  - 1
  - 0.1
  - 0.01
  - 0.001
  - 0.0001
  - 0.00001
  - 0.000001

- **Vgs = -0.1V**
- **V+ = 0V**
- **V- = -5V**
- **TA = +25°C**

**FORWARD TRANSFER CHARACTERISTICS FURTHER EXPANDED (SUBTHRESHOLD)**

- **Vgs = -0.1V**
- **V+ = 0V**
- **V- = -5V**
- **TA = +25°C**
TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

**TRANSCONDUCTANCE vs. AMBIENT TEMPERATURE**

![Graph showing transconductance vs. ambient temperature](image)

**TRANSCONDUCTANCE vs. GATE SOURCE OVERVOLTAGE**

![Graph showing transconductance vs. gate source overvoltage](image)

**TRANSCONDUCTANCE vs. GATE THRESHOLD VOLTAGE**

![Graph showing transconductance vs. gate threshold voltage](image)

**OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE**

![Graph showing output conductance vs. ambient temperature](image)

**ZERO TEMPERATURE COEFFICIENT (ZTC)**

![Graph showing zero temperature coefficient vs. gate source overdrive voltage](image)
TYPICAL APPLICATIONS

LOW VOLTAGE CURRENT SOURCE MIRROR

LOW VOLTAGE CURRENT SOURCE W/ GATE CONTROL

LOW VOLTAGE DIFFERENTIAL AMPLIFIER

V+ = +2.0V to +5.0V

V+ = +5.0V

0.5% PRECISION LOW VOLTAGE CURRENT SOURCE MULTIPLICATION

1/2 ALD1108xx,
1/2 ALD2108xx,
ALD1109xx or
ALD2129xx

M1, M2: N-Channel MOSFET
M3, M4: P-Channel MOSFET

1/2 ALD310708

1/2 ALD310708

M1 M2

1/2 ALD1108xx,
1/2 ALD2108xx,
ALD1109xx or
ALD2129xx

V+ = +5.0V

1/2 ALD1108xx,
1/2 ALD2108xx,
ALD1109xx or
ALD2129xx

A

ALD1108xx or
ALD2108xx

MSET; MN1, MN2, MNX: N-Channel MOSFET

MPSET; MP1, MP2, MPY: P-Channel MOSFET
0.5% LOW VOLTAGE PRECISION CURRENT MIRRORS

\[ V^+ = +2.0V \text{ to } +5.0V \]

\[ \text{ISOURCE} = \text{ISET} = \frac{V^+ - V_t}{R_{\text{SET}}} \]

M1, M2: N-Channel MOSFET

M3, M4: P-Channel MOSFET

0.5% PRECISION LOW VOLTAGE CASCODE CURRENT SOURCES

\[ V^+ = +3.0V \text{ to } +5.0V \]

\[ \text{ISOURCE} = 3 \cdot \text{ISET} = 3 \left( \frac{V^+ - 2V_t}{R_{\text{SET}}} \right) \]

MPA1...MPA4: ALD310708 P-Channel MOSFET (1st individual pkg)

MPB1...MPB4: ALD310708 P-Channel MOSFET (2nd individual pkg)

0.5% PRECISION LOW TEMPCO CASCODE CURRENT SOURCES

\[ V^+ = +3.0V \text{ to } +5.0V \]

\[ \text{ISource} = \text{ISET} = \frac{V^+ - 2V_t}{R_{\text{SET}}} \]

Temperature stable <= 50ppm/°C when ISET = 57µA.
SOIC-16 PACKAGE DRAWING

16 Pin Plastic SOIC Package

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.35</td>
<td>0.053</td>
</tr>
<tr>
<td></td>
<td>1.75</td>
<td>0.069</td>
</tr>
<tr>
<td>A₁</td>
<td>0.10</td>
<td>0.004</td>
</tr>
<tr>
<td></td>
<td>0.25</td>
<td>0.010</td>
</tr>
<tr>
<td>b</td>
<td>0.35</td>
<td>0.014</td>
</tr>
<tr>
<td></td>
<td>0.45</td>
<td>0.018</td>
</tr>
<tr>
<td>C</td>
<td>0.18</td>
<td>0.007</td>
</tr>
<tr>
<td></td>
<td>0.25</td>
<td>0.010</td>
</tr>
<tr>
<td>D-16</td>
<td>9.80</td>
<td>0.385</td>
</tr>
<tr>
<td></td>
<td>10.00</td>
<td>0.394</td>
</tr>
<tr>
<td>E</td>
<td>3.50</td>
<td>0.140</td>
</tr>
<tr>
<td></td>
<td>4.05</td>
<td>0.160</td>
</tr>
<tr>
<td>e</td>
<td>1.27 BSC</td>
<td>0.050 BSC</td>
</tr>
<tr>
<td>H</td>
<td>5.70</td>
<td>0.224</td>
</tr>
<tr>
<td></td>
<td>6.30</td>
<td>0.248</td>
</tr>
<tr>
<td>L</td>
<td>0.60</td>
<td>0.024</td>
</tr>
<tr>
<td></td>
<td>0.937</td>
<td>0.037</td>
</tr>
<tr>
<td>Ø</td>
<td>0°</td>
<td>0°</td>
</tr>
<tr>
<td></td>
<td>8°</td>
<td>8°</td>
</tr>
<tr>
<td>S</td>
<td>0.25</td>
<td>0.010</td>
</tr>
<tr>
<td></td>
<td>0.50</td>
<td>0.020</td>
</tr>
</tbody>
</table>
**PDIP-16 PACKAGE DRAWING**

16 Pin Plastic DIP Package

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.81 - 5.08</td>
<td>0.105 - 0.200</td>
</tr>
<tr>
<td>A₁</td>
<td>0.38 - 1.27</td>
<td>0.015 - 0.050</td>
</tr>
<tr>
<td>A₂</td>
<td>1.27 - 2.03</td>
<td>0.050 - 0.080</td>
</tr>
<tr>
<td>b</td>
<td>0.89 - 1.65</td>
<td>0.035 - 0.065</td>
</tr>
<tr>
<td>b₁</td>
<td>0.38 - 0.51</td>
<td>0.015 - 0.020</td>
</tr>
<tr>
<td>c</td>
<td>0.20 - 0.30</td>
<td>0.008 - 0.012</td>
</tr>
<tr>
<td>D-16</td>
<td>18.93 - 21.33</td>
<td>0.745 - 0.840</td>
</tr>
<tr>
<td>E</td>
<td>5.59 - 7.11</td>
<td>0.220 - 0.280</td>
</tr>
<tr>
<td>E₁</td>
<td>7.62 - 8.26</td>
<td>0.300 - 0.325</td>
</tr>
<tr>
<td>e</td>
<td>2.29 - 2.79</td>
<td>0.090 - 0.110</td>
</tr>
<tr>
<td>e₁</td>
<td>7.37 - 7.87</td>
<td>0.290 - 0.310</td>
</tr>
<tr>
<td>L</td>
<td>2.79 - 3.81</td>
<td>0.110 - 0.150</td>
</tr>
<tr>
<td>S-16</td>
<td>0.38 - 1.52</td>
<td>0.015 - 0.060</td>
</tr>
<tr>
<td>ø</td>
<td>0° - 15°</td>
<td>0° - 15°</td>
</tr>
</tbody>
</table>