

Using Analog CMOS Arrays to Create Current Sources

9.1 RCA pioneered CMOS

Once the first stable MOSFETs had been created in the early 1960s by RCA researchers Steve Hofstein and Fred Heiman, and by Dr. Frank Wanlass at Fairchild Semiconductor, it opened the door to researching and developing other types of MOS transistors. This included small-signal *complementary-MOS* (CMOS) devices, which would theoretically have both N-channel and P-channel transistors coexisting on the same chip together. Although other researchers around the world had tried, no one had yet succeeded in doing this. It was an uncharted area, considered by many to be a lost cause. However, everyone agreed that in theory it was a wonderful concept, particularly for switching functions such as in digital logic gates. The N- and P-channel devices would consume minute amounts of power only during switching (when compared with TTL logic gates), but how to get both types on the same chip was what eluded everyone.

In 1963, Dr. Frank Wanlass at Fairchild Semiconductor discovered that the cause of instability in making MOS devices was trace amounts of sodium. Once the sodium was eliminated, his MOS transistors were perfectly stable. Soon after this discovery, he focused his attention on CMOS, for which he saw a great future. Unfortunately, he could not get his process to work properly because of processing problems. This was a huge technical challenge at the time, but despite not being able to get the device to work properly, he wrote a patent for it anyway. In 1963, Fairchild Semiconductor was granted the first patent for metal-gate CMOS by the U.S. Patent Office. At about the same time, the two RCA researchers, Hofstein and Heiman, developed the first working multitransistor MOS array IC (but not complementary). This in turn led to several government contracts for RCA, for custom MOS devices, although none were made available commercially at the time.

Since the beginning of the 1960s, another small group of researchers at RCA's labs in Princeton, New Jersey, had been researching small-signal MOS devices. They were being pushed by RCA's management to make a breakthrough in this area because it was hoped that MOS would become a viable replacement for some of the vacuum tubes used in its TVs. RCA was primarily a TV set maker. The group, which was managed by Jerry Herzog and led by Israel Kalish, included Al Medwin and Art Lipschutz. Together they developed the first low-power CMOS chip technology and incredibly made the process work, when no one else could. They started by creating simple gates, then decided on a complete digital logic family. At first the devices were speci-

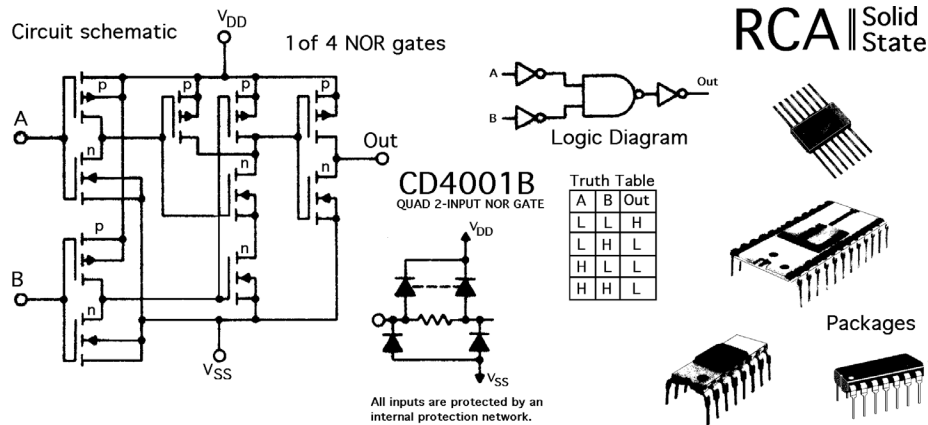


Figure 9.1. When RCA introduced the first commercially available CMOS devices in 1968 it created a whole new facet to the semiconductor industry and was a major milestone in the industry's history. The first devices were simple gates in ceramic flat-packs, then followed ceramic D-I-L packages as shown here.

fied at up to 18-volt operation, but this slowly came down, as their expertise grew. Finally, RCA managed to produce parts that would run on 5-volt (TTL) supplies. When it was ready for the marketplace, RCA called the new technology *complementary symmetry metal-oxide silicon* (abbreviated COS/MOS[®]) and trademarked it.

So in 1968, RCA unveiled its first CMOS logic family, the CD 4000 series (Figure 9.1). Initially it was only available in ceramic packages (like the flat-pack, which the military, NASA, and contractors loved). This introduction was a significant milestone in the marketplace. Up until that time, the logic family of choice had been the bipolar TTL 5400/7400 series, pioneered by Texas Instruments. (TI did not get into CMOS for a long time after it was introduced by National, Motorola, and Fairchild, which quickly shared the new fledgling marketplace with RCA.) Later, others throughout the industry referred to it by the generic name CMOS, which has stuck to this day.

RCA surprisingly had production problems. It was Al Medwin again who found that because most of RCA's production staff were people who had formerly worked with vacuum tubes, they had no concept of handling MOS devices properly or of packaging them. For that reason, Medwin cleverly designed the CMOS family to include built-in input and output protection. It primarily guarded against static *ESD charges* and brief voltage spikes. One major source of problems had been in the packing and shipping area. Now, however, by eliminating static materials from the work area, by much more careful handling and using antistatic packaging, it cured the problem. This little remedy trickled out to the rest of the industry, as it began to license and make CMOS products. It's a procedure that still applies today: always handle CMOS products *care-*

fully, preferably when you are wearing a grounded (via a 1-M Ω resistor) antistatic wristband, on a grounded, static-free work surface.

By the late 1960s, the problems that had previously delayed progress with MOS transistors were all but over. By the early 1970s, the same group of RCA researchers had created more complex products, including the “1801”—the first two-chip CMOS microprocessor developed by Bob Winder. By 1974, another member of the group, Eddie Dingwell, had created the first single-chip CMOS microprocessor, the “1802.” In 1976, Japan’s Hitachi introduced the world’s first complementary power MOSFETs on the same chip, using a proprietary planar, lateral structure. Hitachi followed this just two years later by developing the world’s first fast CMOS devices, in the form of a 4K static CMOS RAM memory chip. It matched the speed of the industry-standard NMOS design (Intel) at the time, but drew only about a tenth of its power. The researcher credited with heading that development was Toshiaki Masuhara, who had been educated at Kyoto University, then later at the University of California at Berkeley. Today he is President of Hitachi Microsystems in Japan.

From the mid-60s through the mid-80s, RCA Solid State, as the division had been named, was a major technology leader in advanced semiconductor devices. Besides the 4000-series logic chips, this included both bipolar discretes (like the famous 2N3055 power transistor), CMOS microprocessor families, CMOS A-to-D converters, the first bipolar-MOS op amps, CMOS A/D “flash” converters, and MOS RF parts. Within a few years, RCA’s CMOS technology was licensed and used by many microprocessor and digital IC makers worldwide. By the early 1970s, RCA’s CMOS devices were being designed into consumer products such as pocket calculators and watches—a huge global market at the time. With this experience in mass-producing CMOS came other technologies and products along the way. This included silicon-gate CMOS, which provided even lower power consumption, smaller chips, and helped open the door for many of today’s battery-powered consumer products.

RCA was eventually absorbed back into General Electric in 1986, and most of its semiconductor portfolio was sold off to Harris Semiconductor. This was part of an even wider reorganization by GE, which later decided to get out of the semiconductor business altogether. Without RCA’s efforts, we probably would not have CMOS as we know it today, where it now dominates various market segments. In the digital marketplace, for example, we have CMOS microprocessors (like Intel’s Pentium™ and Xeon™) and the IBM/Motorola Power PC™ G5 used in today’s Apple Macs, glue-logic, graphics controller chips, and CMOS RAM, to name but a few. In today’s analog marketplace, CMOS op amps, analog switches, A-to-D converters, and power supply controllers are commonplace.

Although RCA had introduced CMOS commercially—first in digital products, then later with analog parts - other companies soon followed. Three U.S. companies that have exclusively pioneered analog CMOS have been Intersil, Maxim Integrated Products, and Advanced Linear Devices. Intersil came first (in 1969) and challenged RCA’s

leadership with several cutting-edge products that included analog switches and op amps. They introduced the first CMOS dual-slope A/D converter (ICL7106), as well as the first CMOS voltage inverter (ICL7660). Both became very popular design-ins and helped further establish analog CMOS products in the marketplace. Intersil's enormous success however resulted in their being acquired by General Electric in 1980. However, this action resulted in the key people who had set up and run Intersil to leave and co-found another CMOS pioneer—Maxim Integrated Products (Sunnyvale, CA), in 1983. Maxim has subsequently established itself as a world leader in analog CMOS with a wide range of products that include op amps, precision voltage references, A/D converters, charge pumps, digital pots, and SMPS products, to name but a few.

When General Electric decided to pull out of the semiconductor business in 1986, it sold off parts of RCA Solid State and Intersil to Harris Semiconductor. Later Harris Corporation decided to spin off its semiconductor operation. Thus Intersil Corporation was reborn in 1999, combining parts of Harris Semiconductor, and GE Solid State. In the ensuing years, it has subsequently grown, and acquired other companies including Elantec Semiconductor, and Xicor Corporation. Today Intersil is ranked in the NASDAQ-100® top companies (as is Maxim), and is once again a global leader in the semiconductor industry. Like Maxim, Intersil also makes a wide range of analog products, and some of the world's most advanced voltage references, that we will read about in Part 2 of this book.

The third analog CMOS pioneer is Advanced Linear Devices (Sunnyvale, CA). Founded in 1985, ALD is probably best known for redesigning the popular "555" timer as a low-voltage, silicon-gate, CMOS device (ALD-555-1), which runs on a miniscule 1-volt supply voltage. ALD also has an exciting range of low-power CMOS products that include op amps, timers, comparators, A/D converters, and electrically programmable analog devices (EPADs® and ETRIMs™), that can be used to build current sources and voltage references. Other major U.S. semiconductor companies with significant analog CMOS product lines today include Analog Devices, National Semiconductor, and Texas Instruments.

The company that has more experience than any other at mass-producing CMOS is National Semiconductor. It was one of the first to begin shipping 74C and 4000-series digital CMOS. For more than 30 years, National has added many other products in CMOS, both digital and analog; some have been simple like a NOR gate, others have been extremely complex, like entire microprocessor families. In addition National has pioneered several A/D and D/A families, as well as CMOS op amps and CMOS voltage references. Today, National Semiconductor is also a world leader in advanced CMOS optical arrays, which are used in some of the the world's most advanced digital cameras, such as those from Hasselblad and Sigma. In a joint venture with Foveon Inc., National co-designs and manufactures CMOS image sensors that are cutting-edge, super-high-resolution technology (more than 16 megapixels), capable of the highest color quality measurable. Yes—National knows all about CMOS too!

9.2 Characteristics of CMOS FETs

CMOS FETs share most of the same characteristics of the low-power enhancement-mode devices DMOS FETs that are described in Chapter 8. However, CMOS designs combine both N-channel and P-channel transistors on the same substrate, whether digital gates or analog op amps. Typically, the N-channel MOS device is used as the driver, while the P-channel transistor is used as its active load. The sensitive inputs and outputs of most CMOS devices employ protective diodes to guard against dangerous static ESD voltage transients. Without this added protection, the ultra-thin oxides used in fabricating CMOS devices can be easily ruptured (see Figure 9.2).

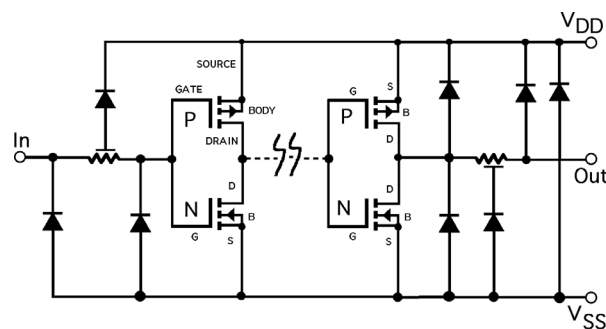


Figure 9.2. CMOS input and output protection networks.

Being low-power enhancement-mode MOSFETs, they are *normally-off* devices and are created as both P-channel or N-channel types on the same substrate. They also have ultra-low current and voltage (low-power) capabilities. In the case of N-channel types, a positive voltage between the gate and source ($+V_{GS}$) is required to turn them on. For the P-channel device, a negative gate-voltage with respect to the source is required to turn it on ($-V_{GS}$). With either polarity of MOSFET, the drain current (I_D) falls to zero when V_{GS} equals 0. CMOS devices use small chips with very low capacitances, resulting in fast (10-nSec) turn-on times.

One major characteristic is that the CMOS FET is a majority-carrier device, which means that it does not suffer from the minority-carrier storage time effect like bipolars do, thereby switching faster. It requires infinitely less gate drive current than a bipolar's average base current or a large MOSFET, and it has a significantly faster switching time—at least five times faster. The CMOS FET also has the ability to be easily paralleled, as well as having a low on-resistance. The resulting lower voltage drop, $V_{DS(on)}$, across the FET translates into much less heat needing to be dissipated from the chip. Last but not least, the CMOS FET's on-resistance, $R_{DS(on)}$, has a positive temperature coefficient. This means that if the FET heats up, its resistance also increases, thereby helping to limit the current through it (the drain current has a negative tempco). This

action reduces the possibility of thermal runaway, as the chip's junction temperature increases.

The symbols, polarities, and large-signal models for both P- and N-channel MOSFETs are shown in Figure 9.3, which is virtually the same as the regular enhancement-mode MOS device. The P-channel MOSFET device shown in Figure 9.3A and B has all of its currents and polarities reversed. CMOS devices have a similar way of operating and share most of the same characteristics and terminology (i.e., $V_{(BR)DSS}$, g_{fs} , $I_{D(off)}$, and I_{GSS}) as the enhancement-mode DMOS FET that we looked at in the previous chapter.

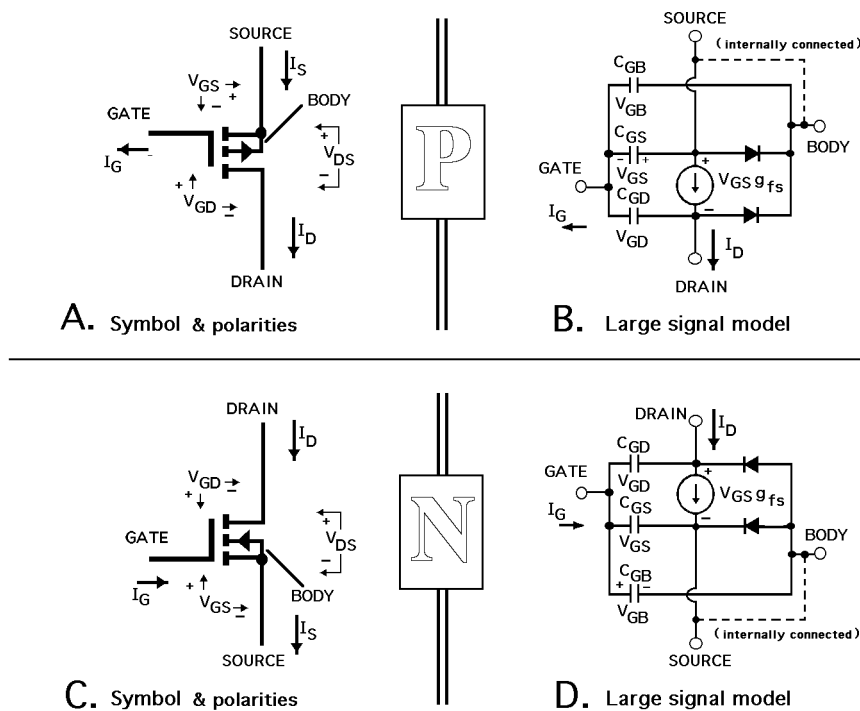


Figure 9.3. Showing the symbols for both P- and N-channel CMOS FETs, as well as various voltages, currents, polarities, and models. Note that for most devices the body terminal is normally tied internally to the source, but not all.

As mentioned previously, enhancement-mode MOSFETs are normally-off devices, requiring either a positive voltage (N-channel types) between the gate and source to turn them on or a negative gate voltage (P-channel types) to turn them on. For either type, biasing the gate to zero volts ($V_{GS} = 0V$) will reduce conduction, until finally a threshold point is reached where conduction ceases. It relies on an isolated, capacitive gate, made with either a metal- or a silicon-gate. An N-channel CMOS

device normally has a very thin oxide layer that isolates the gate from the P-region below. Because the gate is isolated from the rest of the device, it usually has ± 15 -volt limiting gate voltage (some are considerably lower at less than ± 5 volts). By applying a positive drain-to-source voltage of 10 volts and biasing the gate to say 5 volts also in the positive direction, (1) repels the holes away from the surface of the P-region near the gate. This action means that the electrons are now the majority carriers by default, which (2) causes an inversion of the channel (aka surface inversion). (3) This allows electrons to flow in the channel, which induces full conduction between the drain and source. These actions are representative of any N-channel CMOS FET.

P-channel devices work in reverse, by applying a negative drain-to-source voltage (or a more negative voltage) of several volts and biasing the gate to several volts in the negative direction. This first repels the electrons from the N-region near the gate, which allows holes (the majority carriers) to flow in the isolated channel that forms. Again, this induces full conduction between the drain and source. Because P-channel devices are less efficient, they usually require greater chip area to match the characteristics of their N-channel counterparts.

Although one might assume that the typical CMOS FET is a relatively simple device, it actually contains several inherent parasitic elements, which include a bipolar transistor, a JFET, substrate diodes, and various inductances, resistances, and several important capacitances. Each manufacturer uses various proprietary processes to skillfully reduce these unwelcome parasitic characteristics, while exploiting others. The end product is often a compromise between many conflicting characteristics.

An important CMOS FET characteristic regarding its maximum operating voltage is the drain-to-source supply voltage ($V_{(BR)DSS}$). This represents the upper limit of the device's voltage blocking capability and is invariably specified at the beginning of a device's data sheet. Typically, the FET is actually connected to the V_{DD} rail, to which this applies. Although some CMOS devices can work at below 1.5 volts, V_{DD} is more typically between 3 and +12 volts. CMOS devices are manufactured according to a particular process, much of which dictates the breakdown voltage of the device. As a result, CMOS FETs normally use the same value for both $V_{(BR)DSS}$ and $V_{(BR)GSS}$ (the gate-to-source voltage), although the latter is not usually specified other than in the absolute maximum ratings for V_{GS} . Many analog CMOS devices can run on split power supplies (+V and -V) or between 0V and say -10V, so long as $V_{(BR)DSS}$ is never exceeded. As with any type of enhancement-mode device, $V_{(BR)DSS}$ has a positive temperature coefficient of 0.1%/°C.

Although the CMOS FET is controlled by a voltage at its isolated gate, there is actually a very small leakage current involved, called the gate-to-source/body leakage current (I_{GSS}). It is typically in the range of 1 to 50 pico-amps, when measured at room temperature and at a specified gate-to-source voltage. (At elevated temperatures, the leakage current can rise to around 10 nA.) This is measured with the drain terminal shorted to the source and with 10 volts applied between gate and source. The mea-

measurements and levels are virtually identical for both N-channel and P-channel devices. Remember that with most commercially available CMOS FETs, their source and the body regions are internally connected together. This I_{GSS} leakage current doubles for every 10°C rise in temperature, which in some applications may be important. Even so, at 125°C it is almost certainly still below 50 nano-amps, which is quite small.

Another important characteristic is $I_{DS(off)}$, which refers to the small leakage current that flows between drain and source when the gate is shorted to the source (i.e., $V_{GS} = 0$); in other words, when the device is off. This is the same for either N-channel or P-channel devices. At room temperature it is typically a very low value, usually several hundred pico-amps. At elevated temperatures (such as 125°C), it can reach a few microamps. The $I_{DS(off)}$ leakage current is actually that of a reverse-biased diode, and it doubles for every 10°C rise in temperature.

The maximum limiting current that can flow between the CMOS FET's drain and source is known as $I_{DS(on)}$, or the on-state drain current. This occurs at a particular drain-to-source voltage, V_{DS} , and at a particular gate-to-source voltage, V_{GS} (positive value for N-channel and negative value for P-channel devices). The graph depicting this action is shown in the data sheets of all enhancement-mode MOS devices, and as with discretes, it is referred to as the device's *output characteristic* ($I_{DS(on)}$ vs. V_{DS} graph) (see Figure 9.4). When small values of V_{DS} and V_{GS} are simultaneously applied, the drain current increases linearly with V_{DS} . This region is known as the *linear region*. As the V_{DS} is increased, the drain current begins to be pinched off or limited at the knee of the curve, before finally becoming saturated and flattening out. This is known as the *saturation region*. When the drain current reaches saturation, it becomes proportional to the square of the applied V_{GS} , and is then only slightly dependent on V_{DS} ; this is known as $I_{DS(on)}$. Manufacturers usually measure this in a pulse-mode setup, to reduce heating of the chip. With a CMOS FET, this $I_{DS(on)}$ current is usually less than 25 milliamps. It is important to remember that $I_{DS(on)}$ is also limited by the maximum junction temperature, $T_{j(max)}$, which should never be exceeded. Generally, the N-channel device will always have a higher current rating than the P-channel device, and so $I_{DS(on)}$ can typically range 2:1 for complementary devices in the same package. For matched-pairs, however, this is virtually identical. $I_{DS(on)}$ is temperature sensitive and has a negative temperature coefficient of approximately $-0.5\%/^\circ\text{C}$.

Another relevant characteristic of the CMOS FET is its static on-state resistance, $R_{DS(on)}$. For many CMOS FETs, it is often less than $500\ \Omega$. The lower the $R_{DS(on)}$, the higher the current that the device can switch. $R_{DS(on)}$ is measured as the V_{DS} , divided by a particular drain current, at a particular V_{GS} , at 25°C or at an elevated temperature. It can be expressed as:

$$R_{DS(on)} = \frac{V_{DS}}{I_D} \quad (\text{Eq. 9.1})$$

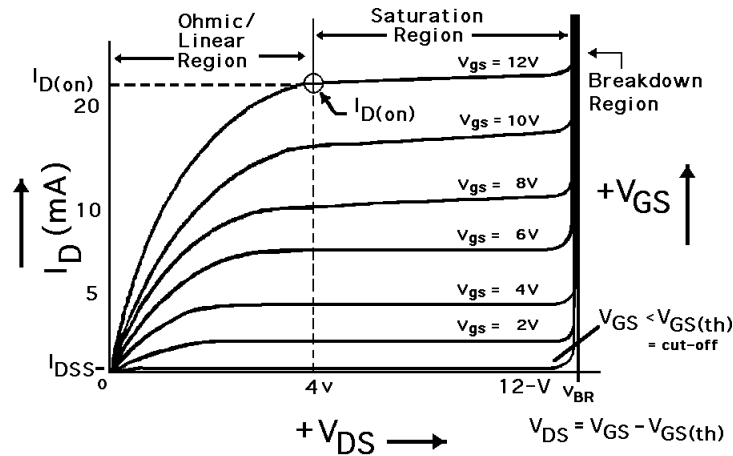


Figure 9.4. Typical output characteristics for an N-channel enhancement-mode CMOS FET.

Because of device self-heating, $R_{DS(on)}$ is usually measured in a pulsed manner, at room temperature, because heating the device decreases carrier mobility, thereby reducing the drain current for a given voltage. At low voltages, $R_{DS(on)}$ is governed mainly by the channel resistance, whereas at higher voltages the epi and JFET regions are most significant. It is interesting to note that the $R_{DS(on)}$ for P-channel devices is typically three to four times higher than for similar N-channel devices on the same substrate. As a result, in order to make complementary pairs with similar on-resistances, the P-channel device needs to be a physically bigger area. With CMOS matched-pairs, a typical figure for $R_{DS(on)}$ mismatching is less than 0.5%. For an N-channel device with a typical $R_{DS(on)}$ of 50 ohms, this would equate to a mismatch of just 250 milli-ohms. For a CMOS FET, $R_{DS(on)}$ has a positive tempco of approximately $+1\%/^{\circ}\text{C}$. Actually, this is a beneficial characteristic, because as the device heats up and the on-resistance increases, the drain current automatically reduces.

Another significant characteristic is the *gate threshold voltage*, $V_{GS(th)}$. This is the gate-to-source threshold voltage necessary to just turn the CMOS FET on, at a very low current level. $V_{GS(th)}$ is actually the voltage required to cause the surface inversion of the channel that allows any forward current to flow. The V_{GS} for an N-channel MOS-FET ranges from 0 volt, where the device is fully cut off, to some positive amount of several volts (typically between 2 and 4 volts) to turn the device fully on. Most CMOS FETs have a very low $V_{GS(th)}$ value, typically ranging between 0.4 and 1 volt. Such devices provide overall faster switching, because less charge current is needed to charge the parasitic input capacitances. However, they are somewhat susceptible to voltage transients, which can cause spurious turn-on of the device. Typically, an analog CMOS FET's isolated gate has ± 8 to ± 15 -volt limiting gate voltage, depending on the device.

Conduction ceases when the V_{GS} drops to less than the threshold voltage; otherwise, the value of V_{GS} mostly controls conduction through the MOSFET's channel. To ensure that the device is fully conducting, a V_{GS} of between +10 volts or higher is recommended for N-channel or -10 volts or more for P-channel. Most enhancement-mode MOSFET data sheets show the drain current I_D vs. V_{GS} curves (aka the transfer characteristic). Manufacturers use a standard drain current of $10 \mu A$ (and with $V_{GS} = V_{DS}$) to determine the $V_{GS(th)}$ value. Manufacturers typically tie the drain and gate together to determine the $V_{GS(th)}$, which is easier to test in a production environment.

Because $V_{GS(th)}$ can typically range over 3:1 for similar devices, it is important that you consider both its minimum and maximum ratings in the range for your application. For dual matched-pairs, this amount is very much closer and typically less than 10 mV. The transfer characteristics show both $I_{D(on)}$ and $V_{GS(th)}$ shift with temperature. Actually, $V_{GS(th)}$ has a negative tempco of approximately $-0.1\%/^{\circ}C$ (approximately $2 \text{ mV}/^{\circ}C$ for each $45^{\circ}C$ rise in junction temperature).

Another characteristic of the CMOS FET is its transconductance/forward conductance (G_{fs}). G_{fs} measures the effect of a change in drain current (I_D), for a specific change in gate voltage (V_{GS}), referenced to common-source mode.

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \Big|_{V_{DS} = \text{constant}} \quad (\text{Eq.9.2})$$

In practical terms, transconductance is a measure of the FET's gain and is a figure of merit. It is usually referred to from a practical standpoint as milliamps per volt (mA/V). On a graph it appears as a steep or shallow slope and is measured and referenced in milli-Siemens (mS). For example, 1 mA/V is a lot more shallow slope than 10 mA/V. G_{fs} is usually specified on the data sheet for some CMOS FETs with a minimum or typical value. The G_{fs} value given in a manufacturer's data sheet is measured at a particular I_D and V_{DS} . Typical values for analog CMOS transistors are between 5 and 10 μS for N-channel FETs and between 2 and 4 μS for P-channel devices.

Another important characteristic of the CMOS FET includes its capacitances. This includes the input capacitance C_{iss} , the output capacitance C_{oss} , and the reverse-transfer capacitance C_{rss} . Of the three, C_{rss} is the most dominating, because it is part of the feedback loop between the device's output and its input. It is also known as the Miller capacitance. The frequency response of the MOSFET is governed by the charging and discharging of C_{iss} , which is composed of the gate-to-source capacitance (C_{GS}), the gate-to-drain capacitance (C_{GD}), and the resistance of the gate overlay structure (not to be confused with the very large input resistance of more than 100 M Ω). This is typically around 20 Ω for silicon-gate and about 10 Ω for metal-gate FETs. Typically, the upper frequency limit of a silicon-gate CMOS FET is in the range of 10 to 50 MHz and about twice that for metal-gate devices. CMOS FETs have a higher frequency response, because the size of the chips is smaller, thereby reducing

the value of C_{iss} . Because C_{iss} is unaffected by temperature effects, neither is the CMOS FET's switching speed.

Remember that a MOSFET has an isolated capacitive gate and that being essentially a capacitor, it takes time to charge or discharge that capacitance, as well as to support a certain amount of charge. It works in the following way: Assuming that an N-channel MOSFET is connected with a 10-volt positive supply voltage at the drain, a source that is grounded, and the gate temporarily at ground, if the gate is now connected to the positive supply voltage, the V_{GS} starts to increase. Soon after it will reach the $V_{GS(th)}$ at say 1.5 volts, at which point a small drain current I_D will start to flow, and the C_{GS} will begin to charge. Once C_{GS} has fully charged, the gate voltage becomes constant and begins to charge the C_{GD} (also known as the Miller capacitance). This takes longer than when charging C_{GS} , because it is a larger capacitance. Once C_{GD} has finished charging, the V_{GS} starts increasing again until it finally reaches the 10-volt supply voltage. When it reaches this point, that is the total time needed to turn the device full-on.

As with all other types of FET, an important characteristic of the CMOS FET is its output conductance (G_{os}). When the FET is applied as a current source, the quality of its current regulation is strongly dependent on its output conductance, which is in turn closely related to its drain current (I_D). The lower the drain current, the lower the conductance, and the better the regulation will be. Remembering that conductance is the reciprocal of resistance, very low conductance translates into high resistance (i.e., a 0.2-mS $g_{os} \approx 5 \text{ K}\Omega$). In practical terms, output conductance is measured and referenced in milli-Siemens (mS). G_{os} is usually specified on the data sheet with a typical value, measured at a particular I_D and V_{DS} .

An important consideration for using any MOSFET is its maximum power dissipation (P_D). While MOSFETs have much better temperature characteristics than bipolars (in that the on-resistance is positive, thus reducing the current flow) and the Safe Operating Area (SOA) is more rectangular, where a bipolar's is more limited, it may still need to dissipate power, in the form of heat, away from the chip. For a CMOS FET, it is limited by its breakdown voltage, current rating, on-resistance, power dissipation, and maximum junction temperature. Exceeding any one of these, particularly its maximum $V_{(BR)DSS}$ rating, could be fatal to the device and the circuit. For CMOS matched-pairs and quads, this specification will probably be around 500 mW, with an operating temperature of 0°C to +70°C. Some devices have a military operating temperature range of -55°C to +125°C.

9.3 Using CMOS linear arrays to create current sources

If you asked most electronic designers how they would create current sources using analog CMOS devices, they would probably tell you that no such devices exist to use in their designs. Wrong! Actually they do exist in the form of various matched-pairs, matched-quads, and matched complementary pairs from Advanced Linear Devices Inc. This Sunnyvale, California-based company specializes in analog CMOS and has an exciting and growing product line. (Most engineers have heard of ALD's super low-

power CMOS “555” timer chip, which runs on an incredible 1 volt.) Besides timer chips, ALD also makes CMOS op amps, A-D converters, comparators, custom ASICs products, and electrically programmable analog devices (EPADs[®]). The ALD products that are particularly suitable for use as current sources are shown in Table 9.1. They are available in various packages, including surface-mount and through-hole, and in either the commercial or military temperature ranges.

ALD’s MOSFET devices are enhancement-mode (normally-off) FETs, manufactured with their proprietary state-of-the-art silicon-gate CMOS process. This process results in creating small, high-speed, very-low-power chips. They are available in several off-set voltage (V_{OS}) grades of between 2 mV and 10 mV. This is the maximum difference in gate-to-source voltage (ΔV_{GS}) between individual transistors on the chip. They offer an extremely high input-impedance, low $R_{DS(on)}$, a fairly low g_{OS} , and very low V_{DS}

ALD Part #:	Description:	Package options:
1101	Dual N-channel matched MOS FET Pair	8-pin TO-99, DIP 8-pin, SO-8
1102	Dual P-channel matched MOS FET Pair	8-pin TO-99, DIP 8-pin, SO-8
1103	Dual N-channel and P-channel matched MOS FET Pair	DIP 14-pin, SO-14
1106	Quad N-channel matched MOS FET Pair	DIP 14-pin, SO-14
1107	Quad P-channel matched MOS FET Pair	DIP 14-pin, SO-14
1108E	Quad N-ch. programmable EPAD [™] Precision matched Pair	CERDIP-16, DIP 16-pin, SOIC-16
1110E	Dual N-ch. programmable EPAD [™] Precision matched Pair	CERDIP-8, DIP 8-pin, SOIC-8
1116	Dual N-channel matched MOS FET Pair	DIP 8-pin, SO-8
1117	Dual P-channel matched MOS FET Pair	DIP 8-pin, SO-8

Table 9.1 ALD’s matched CMOS transistors

operation. They also have low input capacitance (C_{ISS}), therefore fast switching, and have a negative temperature coefficient. These devices all have a guaranteed very low threshold voltage (V_{th}) of 1 volt maximum, for both N-channel *and* P-channel products. Because they are low-power devices, current sources designed with them will be used in designs typically requiring less than 2.5 milliamps. ALD’s EPADs[®] (which we cover later this chapter) are low-voltage, electrically programmable devices that can also be used as precision current sources.

Comparing these devices to JFETs and DMOS FETs that we have looked at previously, these CMOS devices have some major advantages for the designer. First, these devices are matched monolithic pairs or quads, versus unmatched single discrete devices, which one would likely have to try and match in some applications. They definitely provide easier handling and savings, particularly in terms of inventory management and incoming Q&A, not to mention the tedious burn-in, testing, and device matching procedures needed with some discrettes. As a result of the monolithic construction, there is excellent thermal tracking between devices and close matching of

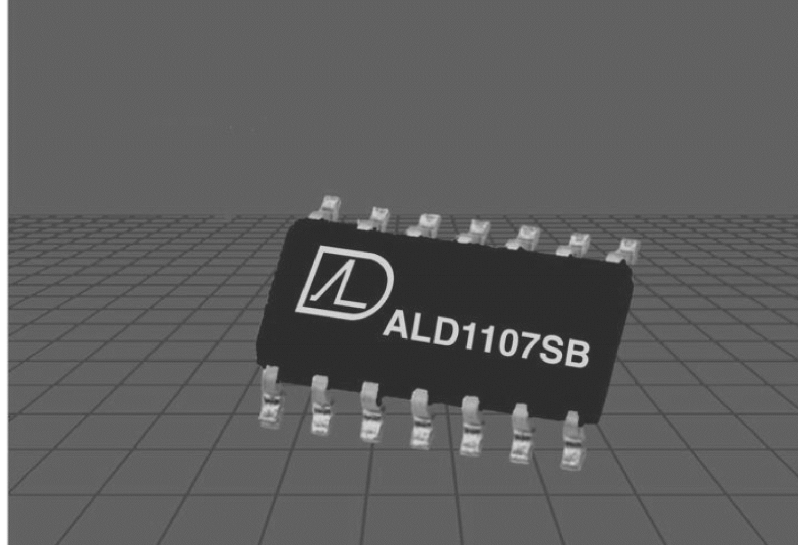
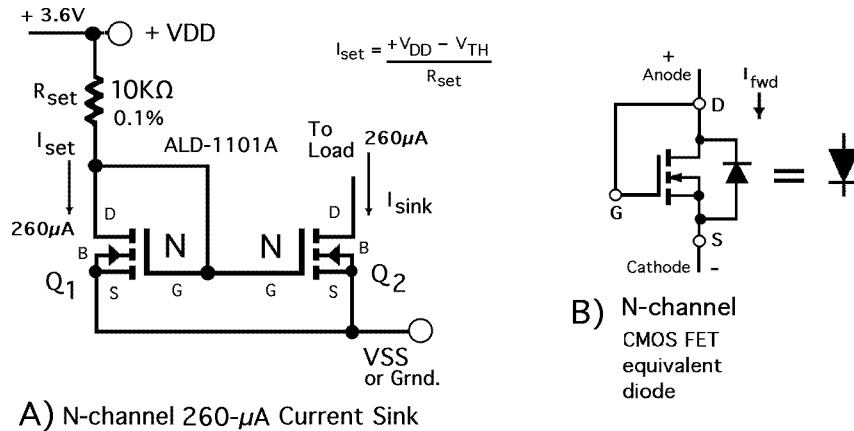


Photo 9.1. Ultra-low threshold CMOS transistor arrays from Advanced Linear Devices, Inc. (Photo courtesy of ALD, Inc.)

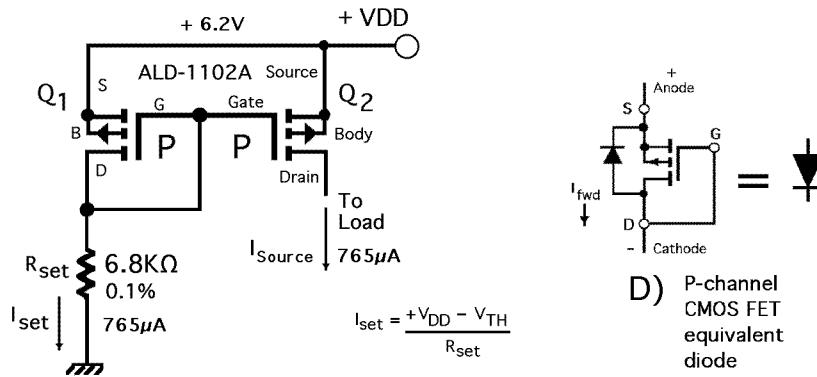
other characteristics. They can provide constant currents over a range of drain-to-source voltages from about 2 volts to 12.5 volts.

One major advantage is that being monolithic duals or quads, they can be made into current mirrors far more easily than discrete FETs. Some practical circuit examples of this are shown in Figures 9.5 to 9.11. As mentioned before, current regulation strongly depends on output conductance (g_{os}), which in turn is closely related to the drain current (I_D). Although in theory a MOSFET may be biased to operate as a current source at any level below its maximum drain current, $I_{D(on)}$, the lower the drain current, the tighter the regulation will be. Best performance is obtained when using a MOSFET that is biased well below its maximum drain current. Because the minimum drain current for ALD's N-channel devices is 30 mA, and for the P-channel devices it is about 11 mA, one should ideally try to make the current source's desired output level 10% or less of either of those values, in order to maximize regulation. While the typical value for output conductance is about 200 μs for the N-channel FETs and about 500 μs for P-channel FETs, a circuit's real output conductance (g_o) will be significantly lower (more than 10 times) than the data sheet value for an individual CMOS transistor (because of a low value of drain current). Cascoding devices (which we will look at shortly) can result in reducing the circuit's output conductance even further (100 times).



A) N-channel 260-µA Current Sink

Using a CMOS N-channel dual matched-pair to create a mirrored current sink. Note the equivalent diode connection.



C) P-channel 765-µA Current Source

Using a CMOS P-channel dual matched-pair to create a mirrored current source. Note the equivalent diode connection.

Figure 9.5. Simple current mirrors using CMOS matched pairs.

Looking at the circuit in Figure 9.5A, this shows a simple current sink using a matched N-channel pair (such as an ALD-1101A). In this circuit transistor Q₁ is

diode-connected (see Figure 9.5B), and as a result the V_{GS} and the transistor's forward transconductance (g_{fs}) control the drain current. This can be shown by:

$$I_D = V_{GS} \cdot g_{fs} \quad (\text{Eq.9.3})$$

If a second transistor (Q_2) is now connected so that its gate and source are in parallel with Q_1 's gate and source, Q_2 's drain current will *mirror* Q_1 's. In this way the mirror current I_{sink} will equal the set current I_{set} . The exact value of current can be determined by the following equation:

$$I_{SET} = \left(\frac{V_{DD} - V_{(TH)}}{R_{SET}} \right) \quad (\text{Eq.9.4})$$

where the gate threshold voltage $V_{(th)}$ is guaranteed to be 1 volt max and V_{DD} is the positive supply. It is assumed that the voltage supply is well-regulated and decoupled with a 0.1- μF disk ceramic capacitor, located close to the current source. In the example shown in Figure 9.5A, a 260- μA current sink is created from a regulated 3.6-volt supply. The resistor R_{SET} should be a good-quality metal-film, 1/4-watt type with a 0.1% tolerance or better and with a low tempco. It is interesting to note that the best performance and regulation occurs when using the MOSFET biased well below its maximum drain current (in this case it is 30 mA minimum). I mentioned previously that one should try to make the current source's desired output level 10% or less of its $I_{DS(on)}$ drain current. In this case, the 260- μA current source equates to just 0.0087% of the minimum $I_{DS(on)}$ value, which would have superb regulation (better than 0.001%).

The circuit in Figure 9.5C shows an ALD-1102A, a matched P-channel pair being used as a simple current source. This circuit works in exactly the same way, except the polarities are reversed, because it uses P-channel FETs. The source current is found by the same formula as in equation 9.4. The equivalent diode-connection for the P-channel connection is shown in Figure 9.5D.

9.3.1 CMOS cascode current sources

Although performance is good using an FET matched-pair, much improved regulation can be achieved by using a *cascode* configuration, as shown in Figure 9.6. Cascoding improves high-frequency operation, provides even greater output impedance (Z_{out}), increases voltage operation and compliance, and reduces output conductance even further. This circuit is a P-channel cascode version of the mirror-pair shown previously in Figure 9.5B and provides even sharper regulation. The operation is essentially the same, except that in this circuit one should remember that *two* gate threshold voltages exist (Q_1 and Q_3 , and Q_2 and Q_4), hence the equation is modified to:

$$I_{SOURCE} = \left(\frac{V_{DD} - 2V_{(TH)}}{R_{SET}} \right) \quad (\text{Eq.9.5})$$

The circuit shown uses the ALD-1107, a monolithic matched P-channel quad transistor array, and as a result good performance can be achieved. Remember too that because the devices all share the same substrate, there will be excellent thermal matching. This quad transistor device is available in either a 14-pin DIP or a 14-pin SO surface-mount package.

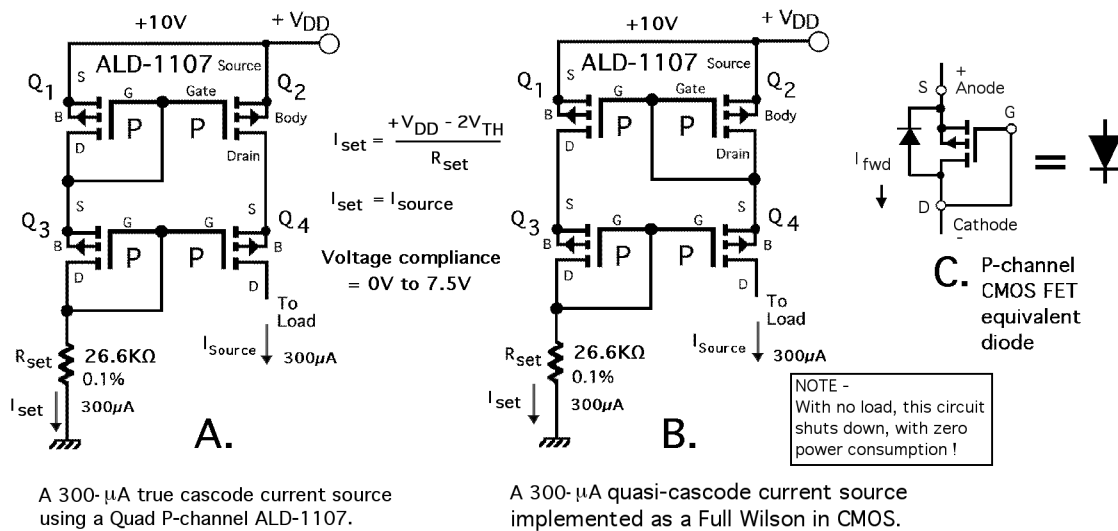


Figure 9.6. Different types of cascode current sources.

The circuits in Figure 9.6 show two different cascode current sources using two matched P-channel pairs (Duals: ALD-1102, 1117; or Quad: ALD-1107). In circuit A, (a true cascode), both Q_1 and Q_3 are diode-connected (Figure 9.6C), and as a result their V_{GS} and their g_{fs} control the drain current. If a third and fourth transistor (Q_2 and Q_4) are now connected so that their gates and sources are in parallel with Q_1 and Q_2 's gates and sources, Q_2 's drain current will mirror Q_1 's. In this way the mirror current I_{source} will equal the set current I_{set} . In this circuit, cascoding buffers the current source from the load, so that variations in the load voltage are accommodated by Q_1 's drain-to-source. As a result the voltage drop across the current source remains constant. Here the drain current (I_D) is regulated by Q_3 and R_{SET} , so that it is mirrored by Q_2 and Q_4 . Both FETs must be operated with adequate V_{DS} , or else the circuit's output conductance will increase significantly. A very low g_{os} value is achieved by either cascode, because of degenerative feedback and the circuit's lower output conductance

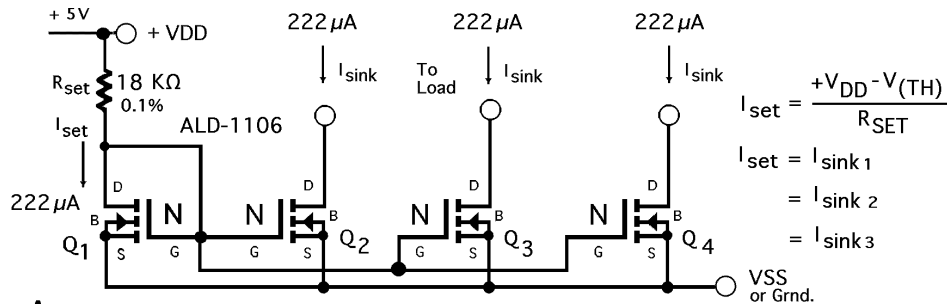
(which in turn is caused by the combined forward transconductance). Here the circuit's output conductance (g_o) is much less than the g_{os} of a single CMOS transistor—about 100 times lower. You can also expect the cascode circuit's minimum output impedance to be more than 100 M Ω , at current levels less than 1 mA, and for best linearity compliance will range from 0 to 7.5 volts. Regulation is at least 10 times better with the cascode circuit.

Figure 9.6B shows a Full Wilson 300- μ A source provided from a 10-volt supply. Here transistors Q_2 and Q_3 are diode-connected, but operation is otherwise similar. One should be aware though that in this circuit, changes in the load (going to high impedance or open-circuit) alter the bias conditions, forcing the circuit to switch *off*. This could be a significant benefit in some applications, where a minimum power dissipation is required. So it is important to remember that this configuration is load-dependent. Again, R_{SET} should be a good-quality metal-film, 1/4-watt type with a 0.1% tolerance or better and with a low tempco. In this case the 300- μ A current source equates to just 0.0272 % of the $I_{DS(on)}$ value, which again would provide superb regulation (better than 0.001%). One could easily use these cascodes in low-voltage circuits of around 2.5 to 5 volts. Ideally, one would like more than 2 volts across each FET, but one can probably get down to a 3-volt supply, because the transistors are ALD's proprietary low-voltage, silicon-gate CMOS devices. These current sources can be built using surface-mount components, taking up minimal circuit board space.

The circuits shown in Figure 9.7 use the ALD-1106, a monolithic matched N-channel quad array. In circuit A, Q_1 and R_{set} determine the 222- μ A current level. Transistors Q_2 through Q_4 mirror this, to provide three slave 222- μ A current sinks. In circuit B, Q_1 and R_{set} again determine the current level, which is set for 750 μ A. Transistors Q_2 through Q_4 mirror the I_{set} current, which is effectively multiplied by the integer (whole number) of additional transistors used in order to create a total I_{sink} current of 2.25 mA. Again, because of the monolithic construction and ALD's close matching, excellent performance in either circuit can be achieved. Notice also that the three CMOS FET transistors are easily paralleled, without regard to base current mismatches or power-hogging, as can occur with BJTs.

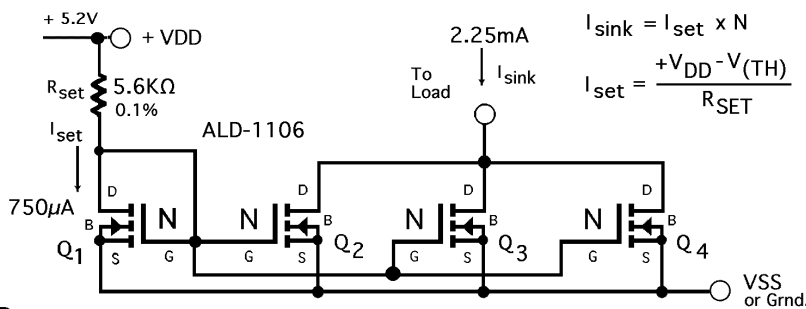
The circuit shown in Figure 9.8 uses the ALD-1107, a monolithic matched P-channel quad array. In this circuit, Q_1 and R_{set} determine the 500- μ A I_{set} current level. This is found by the formula previously shown in equation 9.4 for determining I_{set} . Transistors Q_2 through Q_4 each mirror the I_{set} current, to provide three separate 500- μ A current sources. This popular configuration (two or three P-channel sources) provides optimum performance because of its monolithic construction. It provides excellent thermal matching, as well as close matching of some of its key (amplifier/switch) characteristics (maximum V_{os} equals 2 mV; $\Delta G_{fs} = 0.5\%$ max.; $\Delta R_{DS(on)} = 0.5\%$ max. etc).

This circuit may be easily cascoded, as shown in Figure 9.9. This will provide higher output impedance, higher frequency operation, increased voltage operation, reduced output conductance, and improved regulation. In this circuit, Q_5 and R_{set} determine



A.

A CMOS multiple current sink using an ALD-1106 Quad N-channel array. In this example I_{set} is mirrored by the other transistors in the array.



B.

A CMOS current sink multiplier using an ALD-1106 Quad N-channel array. Here I_{set} is multiplied by the number of mirror-transistors used to determine the value of I_{sink} .

Figure 9.7. Current sinks can be easily implemented with ALD's CMOS arrays.

the $120\text{-}\mu\text{A}$ I_{set} current level. This is found by the formula previously shown in equation 9.5 for determining I_{set} . Transistors Q_6 through Q_8 each mirror the I_{set} current, to provide three separate $120\text{-}\mu\text{A}$ current sources. Operation is essentially the same as shown previously, except that here again remember that *two* gate threshold voltages exist per vertical pair (i.e., Q_1 and Q_5), as per equation 9.5. The cascode circuit shown here uses *two* ALD-1107s, monolithic matched P-channel quad transistor arrays, which are available in either 14-pin DIP or SO surface-mount packages.

Using essentially the same cascoded circuit, one can multiply the separate outputs, as shown in Figure 9.10. In this circuit, Q_5 and R_{set} again determine the $120\text{-}\mu\text{A}$ I_{set} current level. Transistors Q_6 through Q_8 each mirror the I_{set} current, but here the multiplier

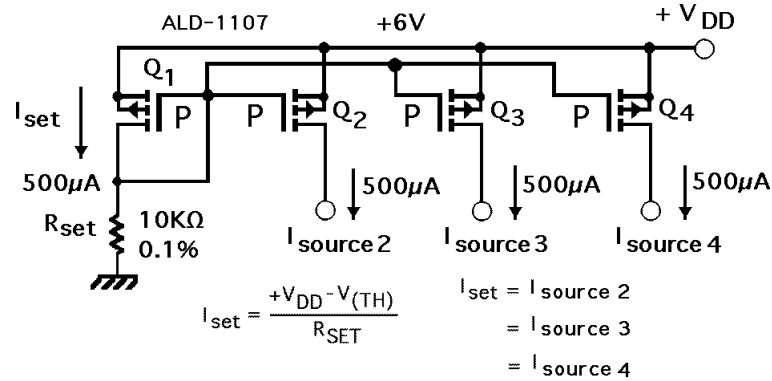


Figure 9.8. A CMOS multiple current source using an ALD-1107 Quad P-channel array.

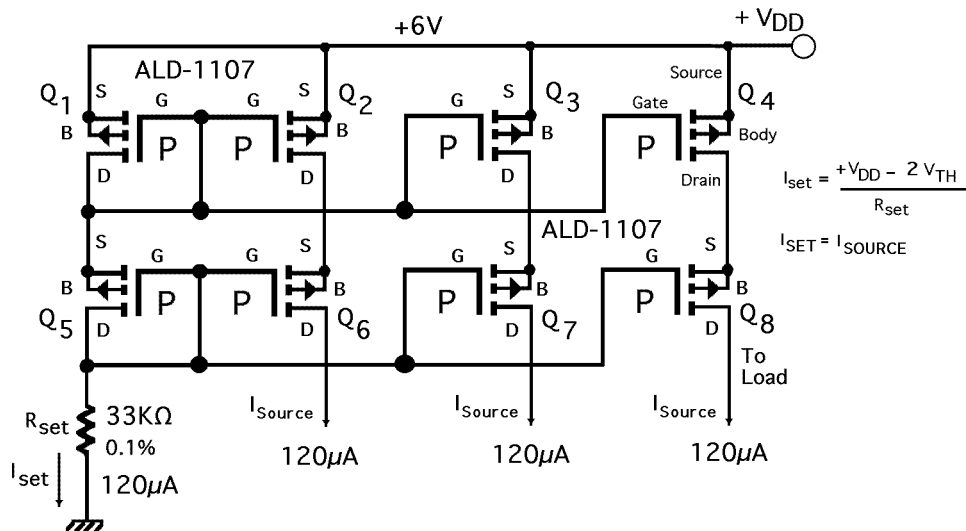


Figure 9.9. Cascoding this multiple current mirror boosts its frequency response, Z_{out} , and regulation.

is three times, which results in a single output current providing $360\ \mu\text{A}$. Operation is otherwise the same, including the *two* gate threshold voltages that exist for each vertical pair (i.e., Q_1 and Q_5), as per equation 9.5. The cascode circuit shown here uses *two* ALD-1107s, monolithic matched P-channel quad transistor arrays.

There are times when a conventional current-source circuit just has to be modified a little to meet the needs of a design application. The circuit shown in Figure 9.11 does

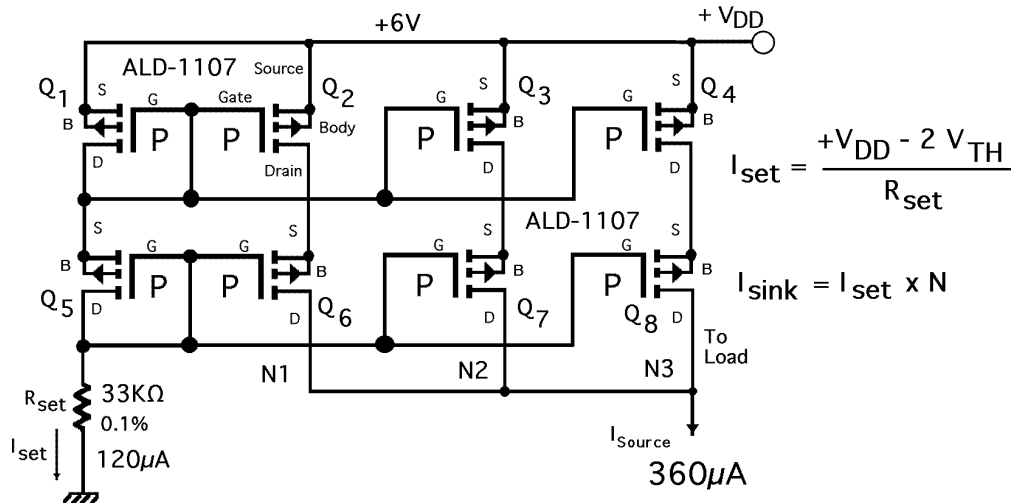


Figure 9.10. A CMOS current multiplier.

such a job by integrating two current sources into a voltage bias scheme. One could imagine that each current source feeds an amplifier stage, with excellent regulation. In this circuit, Q_1 , diodes D_1 to D_4 , and R_1 determine the $200\text{-}\mu\text{A}$ I_{set} current level. The voltage across the diodes will be approximately 2.6 to 2.8 volts and take the place of a transistor for biasing reasons. They each provide negative temperature compensation for the circuit at approximately $2\text{ mV}/^\circ\text{C}$, for a combined total of $8\text{ mV}/^\circ\text{C}$. The voltage drop across Q_1 and diodes D_1 to D_4 needs to be more than 3.8 volts.

The parallel combination of the zener diode ZD_1 , D_5 , and resistor R_2 set up the main biasing for the circuit. The approximate minimum operating voltage for the circuit will be the combined voltage of ZD_1 and D_5 , or else it will not function properly. (In fact, it needs at least 8 volts to function properly). Diode D_5 provides negative temperature compensation for the zener at approximately $2\text{ mV}/^\circ\text{C}$, counteracting the zener's $+5\text{ mV}/^\circ\text{C}$ positive tempco. One can determine the I_{set} value by the following modified formula:

$$I_{\text{SOURCE}} = \left(\frac{V_{\text{DD}} - V_{(\text{TH})} - 2.8\text{V}}{R_{\text{SET}}} \right) \quad (\text{Eq.9.6})$$

Transistors Q_2 through Q_5 each mirror the I_{set} current, to provide two separate $200\text{-}\mu\text{A}$ current sources. Operation is essentially the same as shown previously. This cascode circuit could use both quad and dual P-channel monolithic matched arrays, which could be either in DIP or SO surface-mount packages.

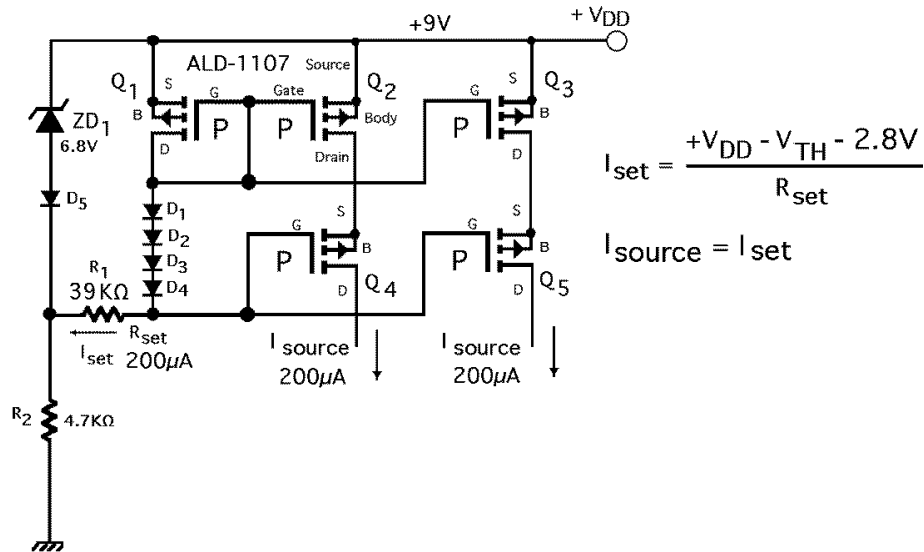


Figure 9.11. Part of the current and voltage biasing circuitry for a typical CMOS op amp. Notice the modified P-channel cascodes, which supply $200\ \mu\text{A}$ to the separate amplifier stages.

You can see another example of how a similarly modified biasing scheme is employed for a typical input stage of a voltage-feedback CMOS op amp in Figure 9.12. It shows how some of ALD's matched CMOS transistor arrays could theoretically be used in order to create one's own op amp. The actual input amplifier stage is created by using a pair of P-channel MOSFETs (in a quad transistor package), while their drain load consists of a pair of N-channel MOSFETs (consisting of the second half of the matched complementary quad), functioning as the current mirror-sink. The zener diode is part of the bias network, working in conjunction with the upper P-channel current mirror-source (in a dual transistor package). This establishes a constant current for the differential amplifier. The drain loads for the differential pair consists of R_3 R_4 , and the mirror sink consisting of Q_5 and Q_6 . The amplifier's offset-voltage (V_{os}) can be adjusted if necessary by connecting a 10-K Ω to 1-M Ω potentiometer across the offset-null terminals. The single-ended output for the following gain stage is provided from the drain of Q_6 . Building such a circuit can provide a great deal of insight into how the op amp's features, such as its input offset-voltage (V_{os}), input offset-voltage drift ($\text{TC}V_{\text{os}}$), low input bias currents, input noise voltage (e_n), slew rate (S_R), input and output voltage range, large signal voltage gain, CMRR, PSRR, power dissipation, supply current, and so on. Luckily for us, ALD makes some excellent CMOS op amps for different applications (high speed, precision, low-voltage operation, and even programmable EPAD[®] op amps), so you don't really need to build your own.

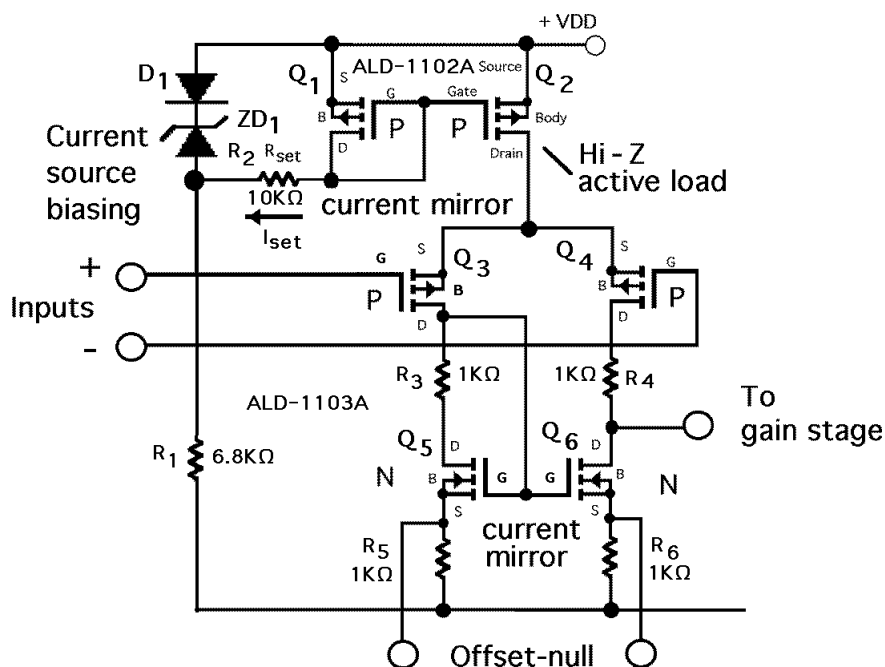


Figure 9.12. Creating a simple op amp front-end amplifier using two pairs of current mirrors to set bias levels.

9.4 Using ALD's programmable EPADs® to create precision current sources

The EPAD® is a kind of analog version of the digital EPROM. Advanced Linear Devices pioneered the electrically programmable analog device (EPAD®) in the late 1990s. Initially, these were matched-pairs and quad transistor arrays, but subsequently they have introduced a whole range of op amps, A/D converters, and other devices. The ALD 1108E (quad) and ALD1110E (dual) precision matched-pairs are examples of this exciting new technology. These CMOS transistor arrays are designed to operate over a 2- to 10-volt supply range and have ultra-low power consumption. They also have a unique electrically programmable gate threshold (V_{th}) feature, which can be easily set by the user. This gate threshold voltage can be set with great precision over a range of between 1 and 3 volts in 100- μ V steps. The initial threshold voltage for new unprogrammed devices is 1.000 volts ($\pm 1\%$). Once set, the device will retain this precise setting for more than 10 years (like a nonvolatile RAM or EPROM), with a drift typically less than 2-mV per 10 years. Such an array, whether quad or dual, can either be programmed in-circuit or with the use of an ALD EPAD® programmer connected to one's PC (see Figure 9.13).

In an OEM environment, it can be programmed on-site before assembly or after assembly as part of a systemwide calibration. With additional circuitry, it can be pro-

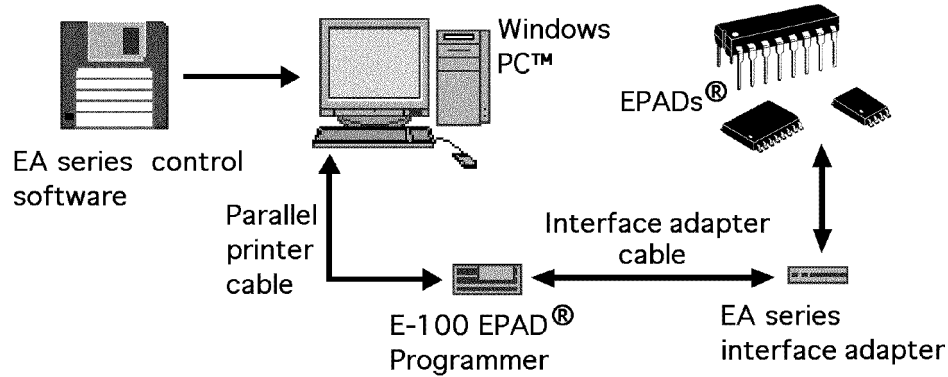


Figure 9.13. A typical EPAD® programming system.

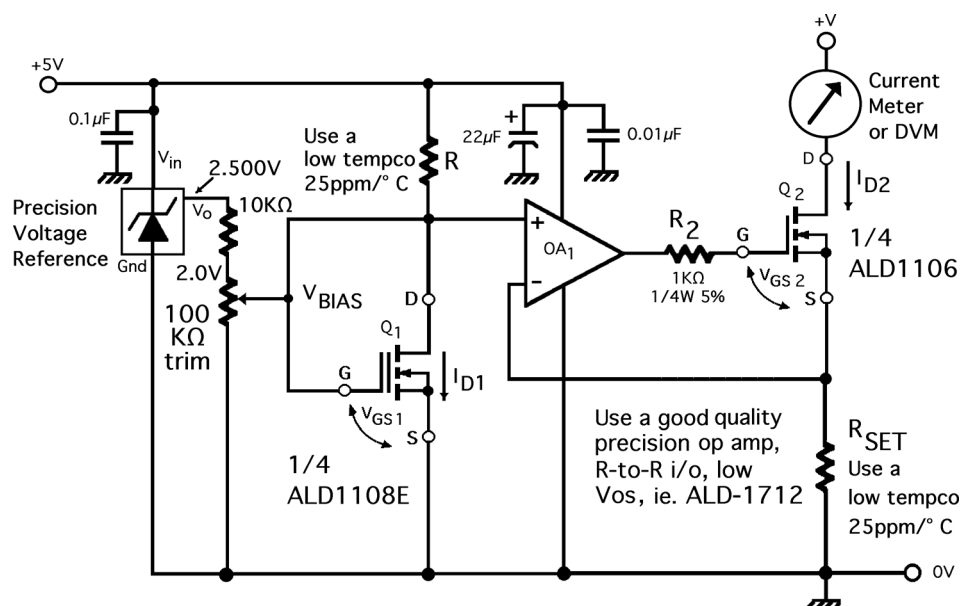
programmed remotely via a network or even over the Internet. This type of device is perfect for manufacturers of potted/sealed assemblies, where trimming or fine calibration is required, or it can be programmed remotely for applications involving hazardous environments or remote locations. The gate threshold voltage can be trimmed, set, and left in a one-time calibration type of application, or it can be increased several times (see Figure 9.14). Once set, the gate threshold setting cannot be reduced or cleared. However, bidirectional adjustments can be made simply by using two devices together with an op amp, where one EPAD® can be made to increase the threshold voltage, while the other uses the op amp to invert the level.

Being N-channel MOS devices, the 1108E and 1110E have very low input currents, and as a result a very high input impedance ($10^{12} \Omega$). Because the gate voltage controls the on-resistance and drain current, either of these characteristics can be effectively trimmed and set as required. Thus, in terms of current sources, they can be programmed to provide a precise constant current over a 100-nA to 3-mA range, and with either a positive, negative, or zero tempco. The devices have a zero tempco current of $68 \mu\text{A}$ over a range of threshold voltages, as seen in Figure 9.15.

Once programmed and set, the devices function like a very-high-quality current sink or current mirror. An example of a current mirror-source using an ALD-1110E EPAD® and an ALD-1102A P-channel MOSFET pair is shown in Figure 9.16.

9.5 ALD breaks the gate-threshold barrier

Advanced Linear Devices introduced some exciting new products in early 2005, which include three new families of precision-matched monolithic pairs and quads. These remarkable ETRIM™ products are based on ALD's well-proven EPAD® technology, but in this case are preprogrammed at the factory in various voltages. What makes these products so attractive is that they have ultra-low gate threshold voltages, typically down to 0.2 volt, and they can run at very low drain-to-source voltages as well. All



Q_1 is the device being programmed, while OA_1 and Q_2 mirror its current, displaying this on the meter. Once you have determined the combination of R and V_{BIAS} , and noted these, you are ready to start programming.

Figure 9.14. Setting up an EPAD[®] precision matched transistor.

of these devices are perfect for battery-powered and portable instrumentation applications. The operating temperature for all of these products is specified for 0° to $+70^\circ\text{C}$. Devices are presently all N-channel transistors and available in either eight-pin DIP or SOIC packages for duals or in either 16-pin DIP or SOIC packages for quads. Because these products are all MOSFET devices, they have a very high input impedance ($1 \times 10^{14} \Omega$), and can provide a very large current gain (1×10^8 ; 100 M) in low-frequency applications. Their maximum gate input leakage current at 25°C is specified at 100 pA, or 1 nA at 125°C , which is also impressive.

One ETRIM[™] family of N-channel precision matched-pairs (ALD110900/A) and quads (ALD110800/A) has a zero-threshold voltage, which eliminates input to output level shifts. These devices have unique characteristics that make them *both* depletion and enhancement types simultaneously. Using these small-signal devices, it has been possible for the first time to build an amplifier input stage that operates from a tiny supply of just 0.2 volt. Another family, the ALD1108xx (quad) and ALD1109xx (dual) precision matched-pairs, are more examples of this exciting new technology. These CMOS enhancement-mode (normally-off) transistor arrays are designed to operate over a 0.2- to 10-volt supply range and have ultra-low $V_{GS(th)}$ voltages. Depending on the

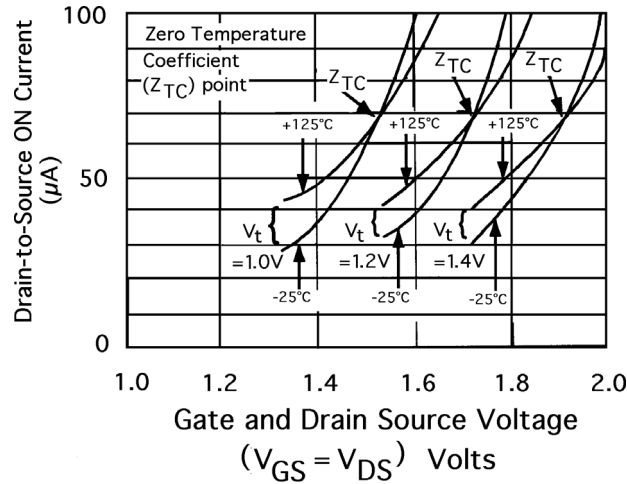


Figure 9.15. The ALD-1108E/1010E EPAD’s drain-to-source ON current, bias current versus ambient temperature.

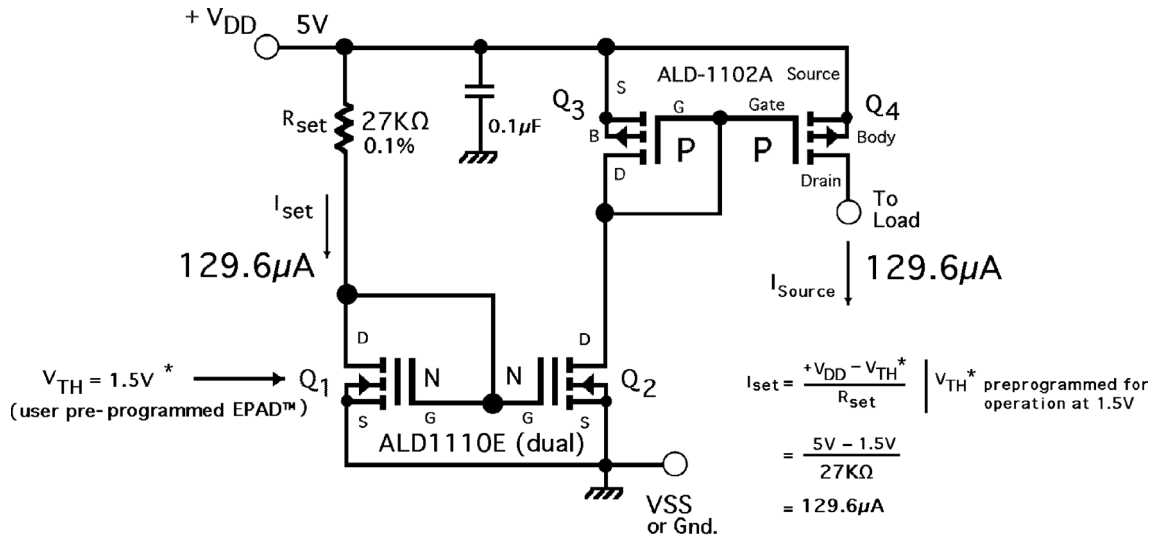


Figure 9.16. A mirror source using an EPAD™ precision-matched pair together with a P-channel MOSFET pair. Note the EPAD™ here has been user programmed for operation at 1.5V_{TH}. Z_{out} is > 10MΩ.

grade chosen, the gate threshold voltage can be as high as 1.42 volt or as low as 0.18 volt (there are four different V_{GS(th)} voltages to choose from), and with different pack-

age options. Once the threshold voltage has been trimmed and set at the factory, the device will retain this precise setting permanently, with a drift of typically less than ± 2 mV/°C.

The third family that ALD is introducing is the ALD1148xx (quads) and ALD1149xx (duals), precision matched-pair devices. These are depletion-mode (normally-on) transistor arrays and are designed to operate over a ± 0.2 - to ± 5 -volt supply range. They too have ultra-low $V_{GS(th)}$ voltages, and depending on the grade chosen, the gate threshold voltage can be as high as -3.5 volt or as low as -0.43 volt (there are also four different $V_{GS(th)}$ voltages to choose from), with two different package options. Being new products, it would be advisable for one to check ALD's Web site (www.ald-inc.com) for the latest information on all of these products.

Such arrays, whether quad or dual devices, can be used to create accurate, low-power current sinks and mirrors, in very-low-voltage applications. Some examples are shown in Figures 9.17 through 9.21. The necessary current-setting design equations are shown in each example. The circuit of Figure 9.17 shows a precision-matched N-channel pair (ALD110902), which is used to create a simple $5\text{-}\mu\text{A}$ current sink, in a circuit running from a minuscule 1-volt supply. With a BJT or JFET current sink, this would not be possible, because in most cases those devices need more operating headroom than the supply voltage here allows.

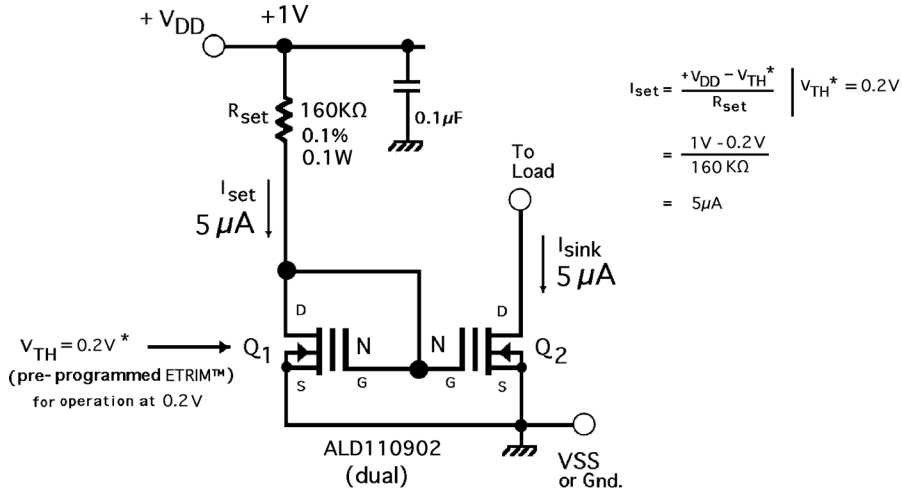


Figure 9.17. A mirror current sink using an ALD ETRIM™ precision-matched N-channel pair. The device has been programmed for operation at a very low gate threshold voltage of 0.2V.

The circuit shown in Figure 9.18 shows an N-channel precision-matched quad (ALD110802), which is used to create a multiple current mirror sink, again with a very low supply voltage (1.2 volt), along with an ultra-low 0.2-volt gate threshold voltage.

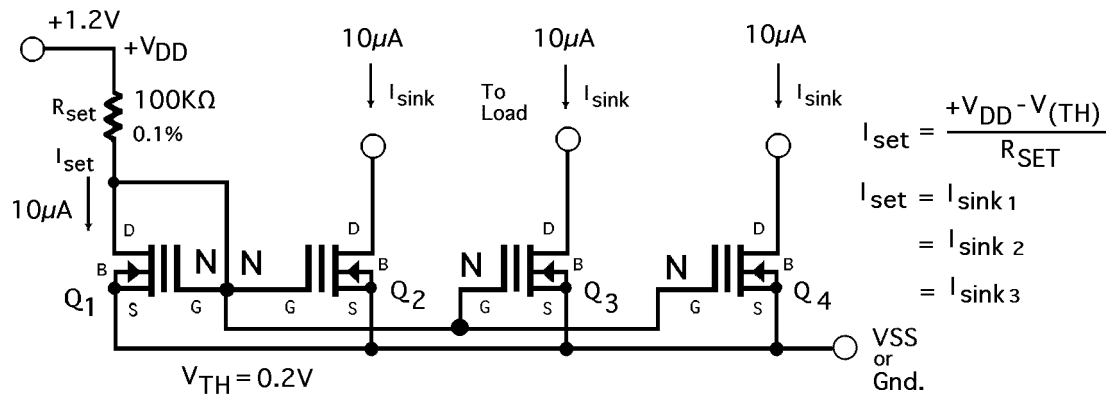


Figure 9.18. A CMOS multiple current sink using an ALD 110802 ETRIM™ ultra-low-threshold, precision-matched, quad N-channel array. In this example I_{set} is mirrored by the other transistors in the array. The supply voltage is a single cell battery.

In Figure 9.19, an e-trimmed N-channel pair (ALD110902A) is combined with a regular ALD-1102 (a matched P-channel dual) to provide a simple current source. The N-channel pair sets the current level, while the P-channel devices mirror this current to the load. The ALD110902A devices in this example have a gate threshold voltage of only 0.2 volt.

Figure 9.20 shows an N-channel matched quad (ALD110802), which is used to create a current sink multiplier, running on an ultra-low supply voltage (0.75 volt). In this circuit, the set current set by Q_1 and R_{set} is mirrored by transistors Q_2 , Q_3 , and Q_4 , but with their drains in parallel. This effectively multiplies the I_{set} current by the number of mirror transistors. This circuit illustrates the importance of having a very low gate threshold voltage, which enables lower voltage operation than is possible with most BJTs, JFETs, or other MOS devices.

The circuit in Figure 9.21 shows two N-channel ETRIM™ transistors using matched array pairs (ALD114904A and ALD110900A), which are used to create a simple current sink. The ALD110900A is a zero-threshold device, while the ALD114904A is a very low threshold depletion-mode (normally-on) device. As a result, this design can run from a very low supply voltage (1 volt). When connected as shown here, the devices can provide a constant current sink of between 5 to 100 μA , with a near-zero tempco.

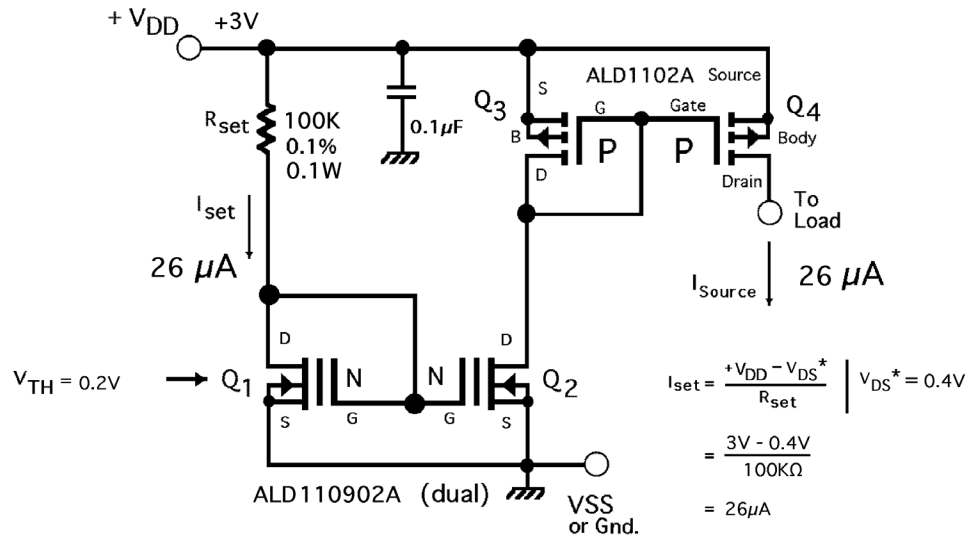


Figure 9.19. A mirror current source using an ALD ETRIM™ precision-matched N-channel pair, with a precision P-channel MOSFET pair. The ETRIM™ has been programmed for operation at a very low 0.20V_{TH}.

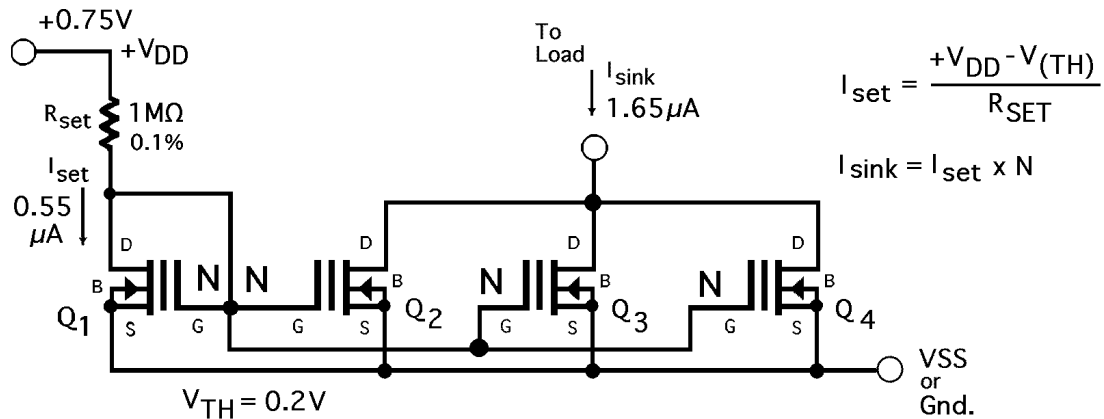


Figure 9.20. A current sink multiplier using an ALD110802 ETRIM™ ultra-low-threshold, quad N-channel array. In this example I_{set} is multiplied by the other transistors. The supply voltage is 0.75V (a typical diode's V_{Fwd}), and the FET's gate V_{TH} is only 0.2V.

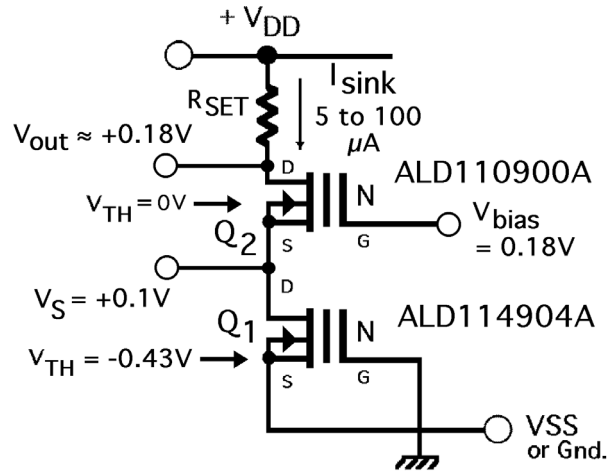


Figure 9.21. A current sink using two ETRIMTM precision-matched N-channel pairs. The devices uniquely provide V_{out} , V_S , and a low current, with a near-zero TC when biased as shown here.

