Category: FET **CIRCUIT IDEAS FOR DESIGNERS** Schematic no. fet_11116.0

Ultra low voltage Nanopower Two-Input NOR and NAND gates

Description

Simple logic gates such as NOR and NAND gates can be readily implemented using EPAD MOSFETs to operate at ultra low voltage and low current levels. At V+ supply voltages below 400 mV, EPAD MOSFETs are actually likely to be always in the "off-state". They are biased and operating with sub-threshold currents, whether in the "1" or the "0" logic state.

Consider the case of a 200mV supply and an EPAD MOSFET with threshold of 0.20V (ALD110802). In the output "1" state, the output is near 0.2V and the EPAD MOSFET is operating in the high end of the sub-threshold region, with drain current of about 230nA. In the output "0" state, the EPAD MOSFET is operating in the low end of the sub-threshold region, with a drain voltage near 0.0V and a drain current of about 19nA. When multiple EPAD MOSFETs are connected to build logic gates, both the "0" state and the "1" state current and voltage levels must satisfy the desired logical output voltage levels and operating temperature range criteria. Laboratory and simulation results indicate that V+= 0.2V is a practical low operating voltage limit for multiple stage logic circuits.