Category: FET

CIRCUIT IDEAS FOR DESIGNERS

Schematic no. fet_11126.0

Single FET Gain Stage

Description

This circuit is a simple common source amplifier. The input impedance is set by RA, the output impedance by RL and the gain is approximately g_m x RL. The bias is set by RS. For currents much lower than $I_D(V_{gs}=0)$ the resistor value is $RS=|V_{th}|/I_{limit}$. One disadvantage of this circuit is that the follower circuit can reduce the gain.

For full schematic diagram and notes, please register and login at aldinc.com

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