Category: Integrators **CIRCUIT IDEAS FOR DESIGNERS** Schematic no. int_42002.0

Differential Integrator with Frequency Controlled Gain

Description

This circuit is a differential integrator circuit with frequency controlled gain. Frequency input is provided by digital clock inputs V_A and V_B, which are out-of-phase non-overlapping digital clocks. The charging capacitor Cs is differentially charged by V_{IN} =V1-V2 during a charge cycle enabled by V_A. Next, V_{IN} is disconnected from Cs when V_A disables (open) the analog switches connected to V_{IN}. V_B is then enabled which connect Cs across the input terminals of the integrating amplifier. Output of the integrator V_{OUT} is determined by the amount of charge on Cs transferred across to the feedback capacitor Cf. The equivalent integration current I_{IN} charges Cf for a fixed time period and produces V_{OUT}. I_{IN} is directly proportional to V_{IN}, and is given by $I_{IN} = V_{IN}/R = V_{OUT} \times Cs \times f$, where f is the switching clock frequency of V_A and V_B. As V_{OUT} is inversely proportional to f, the gain of the circuit is controlled by frequency f. It is important to select an analog switch such as the ALD4201 that has very low charge injection specifications. Analog switch charge-injection caused by its own switching introduces extraneous charge to the charging capacitor Cs and produce errors to the signal on Cs. The non-overlapping clocks V_A and V_B required to drive a quad analog switch such as the ALD4201 can also be replaced with a single clock driving an ALD4213 quad analog switch, which has two normally-closed switches and two normally-open switches in one package.

For full schematic diagram and notes, please register and login at aldinc.com