Description

This circuit uses a matched pair N-channel MOSFET Array (or EPAD MOSFET) for primary temperature and other electrical error effect matching and cancellation. The gate of device 1 and the gate of device 2 are shorted together to ground, thereby forcing both devices to have exactly the same gate bias voltages. The source current through R/2 resistor is equal to drain current of DN1 plus the drain current DN2. At small values of Vo, the drain current of both sides are equal to each other, i.e. Ios1 = Ios2. Depending on the value of R selected, the output Vo is biased in either negative tempco, zero tempco, or positive tempco modes. Note that the resistor R itself also contributes its own tempco term. Interesting variations include using different value for R. By selecting and setting a constant current source level, a voltage output with a certain positive, zero or negative temperature coefficient can be maintained.

For full schematic diagram and notes, please register and login at aldinc.com