Single FET Gain Stage

Description

This circuit is a simple common source amplifier. The input impedance is set by RA, the output impedance by RL and the gain is approximately \( g_m \times RL \). The bias is set by RS. For currents much lower than \( I_D(V_{gs}=0) \) the resistor value is \( RS = |V_{th}|/I_{limit} \). One disadvantage of this circuit is that the follower circuit can reduce the gain.

For full schematic diagram and notes, please register and login at aldinc.com