Description

This voltage clamp circuit produces current versus voltage (I vs. V) that has very sharp turn-on and turn-off characteristics and requires zero power in its off-state. The threshold voltage of the ALD1119xx, V_GS(th) is utilized to control the turn-on voltage of this voltage clamp circuit. At V_GS voltages below V_GS(th), the ALD1119xx MOSFET is turned off and its drain current I_ds decreases exponentially with V_GS decrease.

At V_GS << V_GS(th), the gate of the power PMOS is pulled towards V_DD, turning the power PMOS off. In this state, the quiescent power dissipation of the circuit consists of essentially leakage currents of the ALD1119xx and the power PMOS. When the V_GS (V_GS = V_DD) of the ALD1119xx reaches its V_GS(th), it turns on and conducts current to pull its drain voltage toward GND, thereby turning on the power PMOS as well. The current supplied to load R is limited by the R_DS(on), current of the power PMOS device which, in this example, is about 0.9A. By selecting different values of R_BIAS, the circuit can be turned on at slightly higher (or lower) V_GS from V_GS(th) of the ALD1119xx. This circuit works from about V_DD = 2.0V to V_DD = 5V. For higher voltages from 5V to 10V, it may be necessary to stack two or more ALD1119xx devices on top of each other.

For full schematic diagram and notes, please register and login at aldinc.com