Circuit Ideas for Designers

Schematic no. int_42002.0

Differential Integrator with Frequency Controlled Gain

Description

This circuit is a differential integrator circuit with frequency controlled gain. Frequency input is provided by digital clock inputs VA and VB, which are out-of-phase non-overlapping digital clocks. The charging capacitor Cs is differentially charged by VIN = V1 - V2 during a charge cycle enabled by VA. Next, VIN is disconnected from Cs when VA disables (open) the analog switches connected to VIN. VB is then enabled which connect Cs across the input terminals of the integrating amplifier. Output of the integrator VOUT is determined by the amount of charge on Cs transferred across to the feedback capacitor Cf. The equivalent integration current IIN charges Cf for a fixed time period and produces VOUT. IIN is directly proportional to VIN, and is given by IIN = VIN/R = VOUT x Cs x f, where f is the switching clock frequency of VA and VB. As VOUT is inversely proportional to f, the gain of the circuit is controlled by frequency f. It is important to select an analog switch such as the ALD4201 that has very low charge injection specifications. Analog switch charge-injection caused by its own switching introduces extraneous charge to the charging capacitor Cs and produce errors to the signal on Cs. The non-overlapping clocks VA and VB required to drive a quad analog switch such as the ALD4201 can also be replaced with a single clock driving an ALD4213 quad analog switch, which has two normally-closed switches and two normally-open switches in one package.

For full schematic diagram and notes, please register and login at aldinc.com