Description

Three MOSFETs of a quad supercapacitor auto balancing (SAB) MOSFET array connects across three-supercaps in series, using the ALD 8100xx series, with xx equal to the threshold voltage, $V_t$, in 0.10V increments. At $V_t$, the $I_{DS}$ ON current for each SAB MOSFET M1/M2/M3 is set at 1µA. The $I_{DS}$ ON current of M1/M2/M3 change exponentially with slight changes in the gate-source voltage, $V_{GS}$. Each SAB MOSFET $M_X$ behaves like a voltage sensitive resistor (See sabfet_11101.0). At $V_{GS}$ voltages below or above $V_t$, the SAB MOSFET $I_{DS}$ ON current changes at a rate of approximately 1 decade for every 0.1V change in $V_{GS}$. When $V_{GS}$ drops low enough, the $I_{DS}$ ON current becomes essentially zero. For example, the ALD810025 has a $V_t$ of 2.50V. If its $V_{GS}$ voltage falls below 1.9V, the $I_{DS}$ current decreases to pA range, which is near zero compared to 1µA.

The voltages across M1/M2/M3 automatically self-adjust to accommodate different leakage currents for each supercap C1/C2/C3. $V_1$ and $V_2$ settle to approximately $2/3$ (V+) and $1/3$ (V+) respectively, depending upon relative leakage currents of each supercap in the stack. The currents through M1/M2/M3 automatically compensate for different supercap voltages. A higher supercap voltage results in a higher corresponding $V_{GS}$ voltage of $M_X$ connected across it, at a higher $I_{DS}$ ON current, which opposes the tendency for the higher supercap voltage to increase. A lower supercap voltage results in lower $I_{DS}$ ON currents in the corresponding SAB MOSFET until $I_{DS}$ ON $\approx$ 0. In equilibrium, the total leakage current across both M1/M2/M3 and C1/C2/C3 network is approximately equal to the highest leakage current of any one of C1/C2/C3.

For full schematic diagram and notes, please register and login at aldinc.com