Balancing 2-Supercap Stack with SAB MOSFETs in Parallel

Description
Two supercapacitor auto balancing (SAB) MOSFET array connect in parallel across each supercap of a 2-supercap stack, using a quad ALD 8100xx series, with xx equal to the threshold voltage, $V_t$, in 0.10V increments. At $V_t$, the $I_{DS\text{ ON}}$ current for each of M1/M2/M3/M4 is set at 1µA. The $I_{DS\text{ ON}}$ current of M1/M2/M3/M4 change exponentially with slight changes in the gate-source voltage, $V_{GS}$. Each SAB MOSFET $M_X$ behaves like a voltage sensitive resistor (See sabfet_11101.0). At $V_{GS}$ voltages below or above $V_t$, the SAB MOSFET $I_{DS\text{ ON}}$ current changes at a rate of approximately 1 decade for every 0.1V change in $V_{GS}$. When $V_{GS}$ drops low enough, the $I_{DS\text{ ON}}$ current becomes essentially zero. For example, the ALD810023 has a $V_t$ of 2.30V. If its $V_{GS}$ voltage falls below 1.7V, the $I_{DS\text{ ON}}$ current decreases to pA range, which is near zero compared to 1µA. Connecting two SAB MOSFETs in parallel generally means that two gates, two drains, and two sources are tied together to form a single gate, drain, and source with twice the current running through it. While this increases the leakage current at the standard operating voltage, this configuration increases the maximum charge balancing leakage current at the maximum voltage across the chosen SAB MOSFET.

The voltages across M1/M2 automatically self-adjust to accommodate different leakage currents through C1 and the voltages across M3/M4 automatically self-adjust to accommodate different leakage currents through C2. $V_1$ settles to approximately $\frac{1}{2}$ ($V+$), depending upon relative leakage currents of C1 or C2. The currents through M1/M2/M3/M4 automatically compensate for different supercap voltages. A higher supercap voltage results in a higher corresponding $V_{GS}$ voltage of $M_X$ connected across it, at a higher $I_{DS\text{ ON}}$ current, which opposes the tendency for the higher supercap voltage to increase. A lower supercap voltage results in lower $I_{DS\text{ ON}}$ currents in the corresponding SAB MOSFET until $I_{DS\text{ ON}} \approx 0$. In equilibrium, the total leakage current across both M1/M2/M3/M4 and C1/C2 of each network is approximately equal to the highest leakage current of any one of C1/C2.

For full schematic diagram and notes, please register and login at aldinc.com